Design of Variable and Equal Precision Frequency Measurement Based on CPLD

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Abstract. This paper has proposed an improved frequency conversion equal precision frequency cycle measuring method based on the basic principles of counter cycle measuring method, and it can be used to measure the frequency conversion signal, whose pulse width is much different from repetition period or whose repetition period is random jittering. A high precision real time frequency measurement experiment is completed on CPLD based on the proposed theory and simulation and actual testing have been carried out . The result shows that the proposed system has some advantages of high measurement precision and great real-time performance, and can be widely applied in the field of high precision real time pulse width measurement with low cost.

Introduction

Considering the need of radar to resist the transmission deception jamming, a method of repetition frequency jittering pulse is used. The pulse width of pulse signal in that system is variable in real time, therefore when the signal width is being measured, both the real time performance and the precision of measurement should be taken into account.

There are mainly two methods to measure the frequency of pulse signal at present, namely the frequency measurement method and cycle measurement method [1]. As for frequency measurement method, its schematic is to count the measured signal in unit interval, and for cycle measurement method, its schematic is to count the reference pulse in the period of measured signal[2]. The difference of the two methods is whether the counted object is measured signal or the reference pulse supplied by system. The main disadvantage of both the two methods is that the measurement error will be larger when the frequency changes a lot. To solve the problem[3-5], this paper proposes a new method called variable and equal precision frequency measurement , it can adjust the reference clock according to the variety of measurement frequency automatically and in real time, achieving the aims of equal precision and real time measurement, the specific realization method and the actual measurement results analysis are also given in this paper.

Schematic of variable and equal precision frequency measurement method

The schematic of equal precision measurement can be summarized as follow. Based on cycle measurement method, then a counter uses reference pulse to count the measured pulse, if the counter overflows in one measured period, the frequency should be reduced by the method in situation one mentioned above and then go on with the measurement until complete the counting for pulse width of measured signal. There will be three advantages to do so. One is that the real time problem of measurement is solved, and each pulse width of measured signal can be measured alone; the second is that the counter digits are limited and the system resource is under control. This can be widely applied in the design project whose needs for counter digits and data transmission and data storage is not very high; The third one is that equal precision measurement is realized with little system resource and the measurement error is also controlled within a proper range.

Design and implementation based on CPLD

To realize the schematic of proposed equal precision frequency measurement, the key is to solve the problem of changing reference frequency according to the changing period of measured signal.A method based on state computer has been applied here, which can count the reference pulse in a measured period, and give the overflow signal of the counter to change the operation of state computer, so as to change the frequency of reference pulse (decrease the frequency of reference pulse), frequency changing module can supply the various frequency signals needed by state computer. The schematic of design is showed in Fig.1.

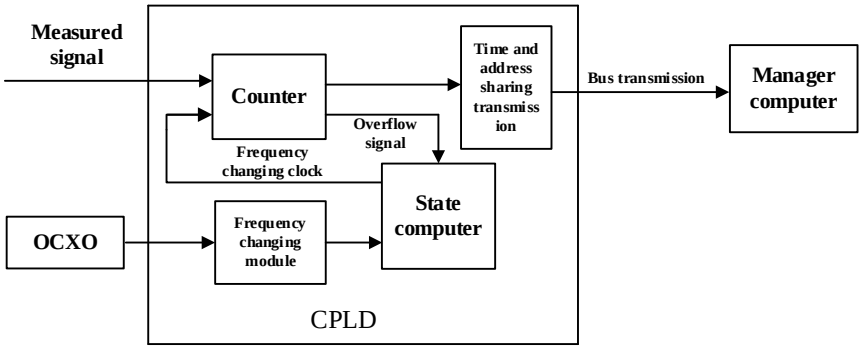

Fig.1 Schematic of pulse envelope equal precision measurement method

Suppose that the width of pulse envelope send by radar is 0.5us to 50us, the repetition period is 50Hz to 5000Hz, and the measurement error should be less than 1%. According to the requirements, EPM1270T144 of MXAII series[1] is selected in CPLD, the crystal oscillator is a constant temperature crystal oscillator with a frequency of 100MHz to ensure the measurement precision. Considering that VHDL, a kind of hardware description languages, is selected to develop CPLD, and the convenience for parallel transmission of data, a binary counter is selected. The modules of CPLD are illustrated below.

Counter module designing. As the design of counter is the core of the whole system, to measure the pulse width and period in one period, this paper uses a method of countering the high level and low level of a periodic pulse separately. The high level width that we measured is the pulse width;the sum of high level width and low level width is the period. Because the rising edge and falling edge cannot be detected in one process in VHDL[2], to count the high level width of measured signal, the counting must start at the time that high level comes, and stop at the time that falling edge comes,and it is also the same for falling edge measurement. To solve the problem in programming, here two counters, namely “count1” and “count2”are designed. The function of “count1” is to count the high level, and the function of “count2” is to count the low level, they can work in parallel and without interference, therefore each period can be measured and the problem of real time measurement has been solved.

Frequency changing module designing. According to the difference of frequency changing clock, this module is designed to have four states, namely S1, S2, S3 and error. When the signal “state_over” sent by counter is “00”, this module comes into state S1, at the same time output of frequency changing reference clock “clk_change” is 100MHz, supplying the reference counting clock for counter. If “state_over” is “01”, the module converts to state S2, the output of “clk_change” converts to a 16 fractional frequency of 100MHz. If “state_over” is “10”, the module converts to state S3, the output of “clk_change” changes to a 256 fractional frequency of 100MHz. If “state_over” is “11”, the module changes to error state, the output of “clk_change” converts to 0. The measurement range can be calculated according to the reference clock of different states, for instance, in state S1, if overflow happens when counting a reference clock of 100MHz (the counting number is lager than 8192), a overflow signal will be sent by counter, and then the state changes to S2. The upper limit of measurement in state S1 is 100MHz/213=12.2kHz, the other state measurement range can be calculated in the same way.

Frequency changing clock module designing. As measuring frequency with different measurement range needs different reference signal, the frequency changing clock module is

necessary, since it can supply the needed reference clock after the state of counter changes. In detail, the fractional frequency module has divided the frequency of 100MHz by 16 twice, and generated three clock signals for state computer including 100MHz.

Analysis of experiment results

Firstly, the whole design is simulated by software. Fixed frequency is measured by simulation for the three state measurement ranges separately, to prove that variable frequency equal precision measuring is feasible and within an acceptable measurement error range.

When repetition period is being measured, firstly the pulse width of low level should be measured, and added by width of high level signal. The sum is width of the period. The width of low level is measured by counter 2 with four pulse widths at different state ranges, namely 100us, 1000us, 1400us and 20000us.

The total simulation result is showed in table 1. The results show that all the errors are within the acceptable in different measurement range.

Tab.1 Analysis and comparison of the simulation results

Measurement range	Pulse width	Simulation results	Relative error
S_1:0~81.92us	0.5us	0.49	2%
	50us	49.99	0.02%
S_2:81.92us~1310.72us	100us	100.00	<1%
	1000us	1000.00	<1%
S_3:1310.72us~20971.52	1400us	1400.32	<1%
us	20000us	19998.72	<1%

Now based on the perfect simulation results, an actual measurement is carried out. The measured signal is a square wave generated in given measurement range by Agilent 33521A single channel function and arbitrary wave generator together. The frequency range of Agilent 33521A is from 1uHz to 30MHz with a resolution of 1uHz and harmonic distortion lower than 0.04%. The test results is showed in table 2.

Tab.2 Actual measurement results

State	Width of measured pulse	Measurement results	Relative error
S_1:0~81.92us	0.5us	0.49us	2%
	50us	49.89us	0.22%
S_2:81.92us~1310.72us	100us	99.98us	0.02%
	1000us	999.99	<1%
S_3:1310.72us~20971.52	1400us	1399.97	<1%
us	20000us	20000.50	<1%

According to table 4, the actual measurement result is totally the same as the simulation result. As for relative error, all are acceptable except the error of measurement in point 0.5us.

Conclusion

This paper has proposed an advanced variable frequency equal precision measurement method based on the schematic of cycle measurement method, and realizes accurate measuring of pulse width on CPLD, and in the design of which the requirement of counter digits and data transmission and data storage is not very high, the proposed method can be used to measure the frequency conversion signal whose pulse width is much different from repetition period or whose repetition period is random jittering. The simulation and the result show that the proposed method can achieve the aim of accurate measuring of the pulse width of radar signal.

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