Multifunctional readout circuit design of infrared detector

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Keywords: FEDI; H-CTIA; Linearity; SNR; Weak signal

Abstract. The new dual-band infrared detector can be read out to design a weak signal readout circuit, the readout circuit integration time is adjustable, and has characteristics of low power consumption, low noise and high sensitivity.Using feedback enhanced direct injection readout circuit (FEDI) and high performance capacitive feedback transimpedance amplifier (H-CTIA) combining circuit pattern structure, and the switch circuit is adjusted by way of two adjacent pixels ,which share one of the amplifier circuit. This not only reduces the area which is occupied by an amplifier in the single pixel circuit, but also reduces the complexity of the circuit design. By integrating capacitor circuit and adjusting the sampling capacitor, the readout circuit can be achieved after the first integrator output mode and the side edge integral output mode. Combined with complementary S matrix coding regulatory principles to eliminate stray light circuit dark current noise, ultimately it can read out weak signals. In this study, TSMC 0.35um 2P4M technology taped the circuit area of the synthesized pixel unit of 35um × 35um, entered the photocurrent is 0.09pA ~ 48nA, the output signal to noise ratio can reach 72dB, high linearity response to 99.3%, ROIC accuracy has been greatly improved, which can meet the desired designing requirements.

Introduction

In recent years, with the advancement of science and technology, infrared detectors have caused people's particular concern. The design of ROIC is the most important part of the infrared focal plane array structure, it's also the bridge of analog and digital signal.

For blackbody radiation surrounding objects,photocurrent signal radiation is very small.Photocurrent size is only nanoamp or picoamp level,it's very difficult to readout such a small signal. Simultaneously, in the use of the engineering,

Miniaturized circuit design requirements are also increasing. So it need to design a infrared detector circuit which can readout weak signals and the occupied area of this circuit must be moderate[1-4].

At present,the more commonly used pixel circuit structure are the current mirror circuit integral type, DI injection enhanced feedback structure and high-performance capacitive feedback transimpedance amplifier structure.DI injection enhanced feedback structure is relatively simple, small size,power consumption is very low,wide linear response range and input impedance is very small,and the readout circuit current is smaller than the H-CTIA circuit.High performance capacitive feedback transimpedance amplifier architecture provides a very low input impedance detector and a constant bias voltage detector,the output signal linearity and unifornity is also very good[5-6].The design of the FEDI and CTIA structure were conbined to achieve dual pixel circuit design,and post-stage circuit,increasing the integration time adjustable design, making more flexible readout circuit. according to the detector usage, making specific adjustments by controlling the switch.

By introducing the principle of complementarity S matrix coding[7] adjustment to remove stray light noise and dark current noise,thus it can improve the overall performance of the readout circuit.

1.Critical circuit design elements

1.1 Dual pixel circuit

To design a novel dual detector pixel circuit,the dual-mode cell circuits mixed with H-CTIA and FEDI architecture,combined into one pixel units,each pixel unit has two modes to operate.In order to reduce the area of the circuit design,the amplifier is placed between two adjacent pixels,thus it's possible to reduce the area which is occupied by the amplifier in the single pixel circuit.Figure 1 is the pixel mode switching circuit.

In order to meet the different infrared detector,the cell stucture of the circuit can be used to adjust the switches G1 and G2.We can use semi-loop technology to put the difference between the two structure of the FEDI readout circuit,so that the two sides readout circuit has the same differential circuit.When the switch of G2 is closed,the switch of G1 is opening,the pixel's condition is in FEDI mode， the FEDI circuit current can be readout smaller than H-CTIA circuit.When the switch of G1 is turned off,the switch of G2 is opening,the pixel's condition is in H-CTIA mode.

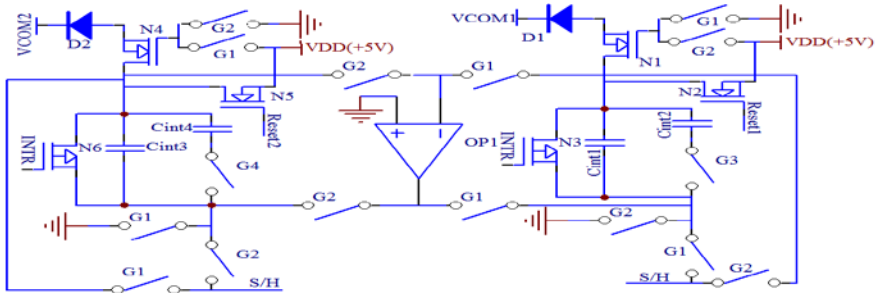


Fig.1:Two-mode pixel circuit frame as a whole

For photocurrent is relatively large ,and the change is also a wide range of circumtances, the use of two parallel capacitors to adjust the injection efficiency.In both architechure mode,when injected into the photocurrent is small,don't turn on the switch G3(or G4),the integrating capacitor just use Cint1(or Cint3) to meet the requirements.When the injection current is large,you need to turn off the switch G3(or G4),this time with the intergrating capacitor values and Cint1(or Cint3)with Cint2(or Cint4) capacitance value and the capacitance value,thus extending the intergration time,increase the charge capacity.When switching to FEDI architecture patterns,photocurrent injected into the integration capacitor, the integration voltage is proportional with integral time,also the input current is a constant value,so the output of the integrator signal at this time is:

$$V_{FEDI} = \frac{I \times \mathrm{T}_{\mathrm{int}}}{C_{\mathrm{int}}} \tag{1}$$

When switched to the H-CTIA architecture model,the circuit is in the integral state,the current though the light integrating capacitor,so that the integrating capacitor is charged.Integrating capacitor voltage increases,the output voltage decreases cell,so H-CTIA mode output voltage is reduced.In this process,it is related to the bias voltage,the charging process can be expressed as:

$$V_{H-CTIA} = V_{bias} - \frac{I \times T_{\mathrm{int}}}{C_{\mathrm{int}}} \tag{2}$$

Wherein, Tint represents the integration time, I represents photocurrent.

1.2 Sample with hold and pixel signal output circuit

Figure2 is given by the sample with hold output signal and the pixel circuit architecture.By control K,the dual pixel circuit integration capacitor voltage signals can be collected in the capacitor C1.Separating of the intergrating circuit in FIG.1 and the sample with hold circuit in FIG.2, the circuit can be realized integral side edge after the first intergrator output mode and output mode.

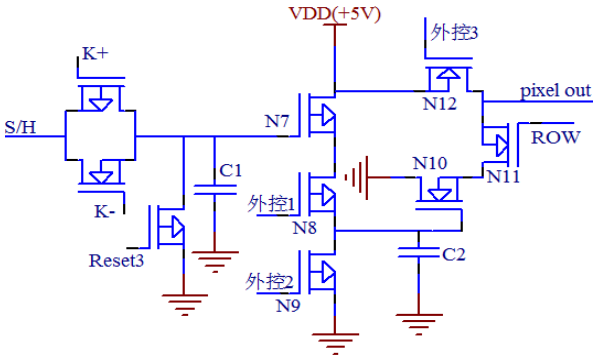


Fig.2:Sample with hold circuit and pixel signal output

Integral side edge output mode

conjunctting with Figure 1, we can select any one mode in the dual-mode pixel circuit, and turn off the switch of G3 (or G4), then reset these two high-level integration capacitor ,start the integration at last; Again to Figure 2,capacitor C1 is low reset,when the resetting is completed,we need to shut K. In this case, you can put two integrator capacitor voltage signal of one mode of the two dual pixels circuit to the capacitor C1,the sampled voltage value can be expressed as:

$$U_{\mathrm{M}}=\frac{U_{C_a+C_b}(C_a+C_b)+I_{opt}T}{C_a+C_b+C1} \tag{3}$$

Wherein, Iopt and T each represent photocurrent and sampling time， UCa +Cb

represents the dual pixel circuit in Figure 1, one of two modes integrated voltage capacitor.UM represents the sampling voltage in the capacitor C1 in Fig. 2. Ca represents Cint1 (or Cint2), Cb represents Cint3 (or Cint4). By the above formula we can know, in this mode, the circuit output swing fell after sampling C1/(Ca +Cb+ C1), After the charge is transferred to C1, and subsequent circuit schematic, it can read-out the signal at the final. Thereafter, each capacitor is resetted, integratted, and sampled.It can output the signal at last.

In this mode, the time is relatively abundant, the integration phase and sampling stage acomplish their work, so it can quickly output the pixel signal.

After the first integrator output mode

When combined with Figure 1, in the dual-mode pixel circuit, we can select the FEDI (or H-CTIA) mode, close the switch G3 (or G4), plus the capacitors C1 in Figure 2, so these three parallel capacitor can be used as an intergrating capacitor . then it can achieve the longest integration time. At this time, the integrator stage and the output stage are separated, so the interference between them is reduced, and the noise signal is reduced.

1.3 ROIC SNR main influencing factors

Since the output signal has a second harmonic impact[8],we can contrast the stray light noise and dark current noise with this harmonic.on account of

$Q\bar{i}BR<<\bar{i}S_{REC}^2M$, Wherein R is the structure of the two modes of cross-resistance,M is the local oscillation light amplitude, SREC is the area of the incident light received by the detector[9]. Over the entire bandwidth, power spectral density is evenly distributed. And stray light and dark current noise current can be expressed as:

$$I_{\mathrm{ZS}}=2Q\bar{i}B \tag{4}$$

Wherein, $\bar{i}$ represents the average value of the photocurrent on the sensor;Q represents the amount of charge;B indicates the bandwidth. It can be seen that the main noise of the structure is stray light and dark current noise.

2.Simulation and Test Results

2.1Separation of signal and noise

The design uses a complementary S matrix coding regulatory principles [10] to eliminate the effects of stray light and dark current noise. Using this principle of the circuit modulation spectroscopy, measured, can be obtained spectrum signal is:

$$S_1 = \sum_{n} U_{mn}^{+}(y_n) + F_m + H_m \tag{5}$$

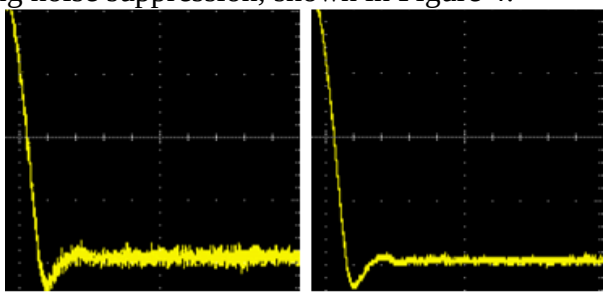
Wherein: the encoding matrix is represented by Umn+; dark current noise is represented by Hm; spurious noise is represented by Fm; spectrum signal is represented by yn. S matrix coding adjustment in accordance with the principle of complementarity to modulation spectroscopy, spectral signal measured can be expressed as:

$$S_2 = \sum_{n} U_{mn}^{-}(y_n) + F_m + H_m \tag{6}$$

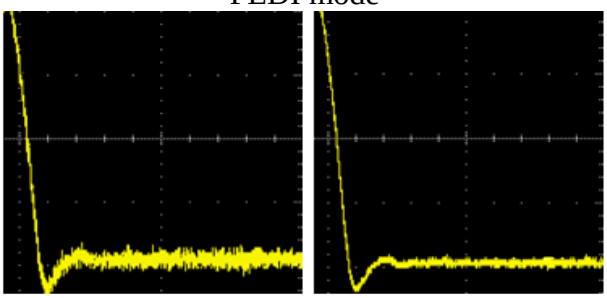
The (5) and (6) two subtraction, we can get:

$$S = \sum_{n} U_{K_{mn}}(y_n) \tag{7}$$

It can be seen, the stray light noise and dark current noise can be eliminated. For FEDI and H-CTIA two modes, the use of this principle, by simulation,we can get the output signal waveform before and after suppressing noise suppression, shown in Figure 4:



FEDI mode



H-CTIA mode

Fig.3:The output signal waveform before and after noise suppression in either mode

SNR calculation formula can be expressed as:SNR=E_t/RW,RW represents the noise equivalent power density, Et represents irradiance. You can enhance the signal to noise ratio 2.33 times and 2.30 times, respectively, in both modes, calculated SNR up to 72dB.

2.2After dark current and preamplifier circuit integrating capacitor relations

In FEDI with CTIA mode, post-stage amplifier circuit and the integrating capacitor readout dark current relationship is shown in Figure 5, wherein in response to the voltage saturation point represented by V0.

In the circuit, the two capacitors of C3 and C4 were taken 3pF and 9pF, after the combination switch control, there are three possible capacitance value, the capacitance values of these three were 3pF, 9pF and 12pF, 3 rectangular integrating capacitance, respectively said shading indicates the dark current value integrating capacitor respectively occupied, a blank portion represents also read

the response threshold voltage, can be seen from the figure, the smaller the integration capacitor, the greater the response integral reading voltage threshold.

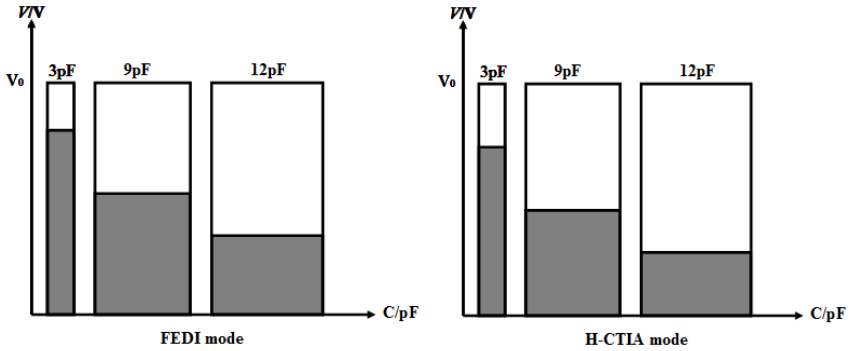


Fig.4:The relationship between capacitance and dark current when the read voltage saturation point is identical

2.3Measuring the relationship between the input current and output chip voltage

At room temperature conditions, given the different input current value and the integration time 64us, the measuring tip of the input current and output voltage relationship corresponding to different modes, can be seen from Figure 5, in FEDI mode, the voltage at 1.7V to 3.7V, output voltage swing near 2V; when H-CTIA mode, the voltage of 3V to 1.7V, the output voltage swing near 1.3V. The gradient of the output voltage is calculated, the linearity can be obtained in both modes are above 99.3%.

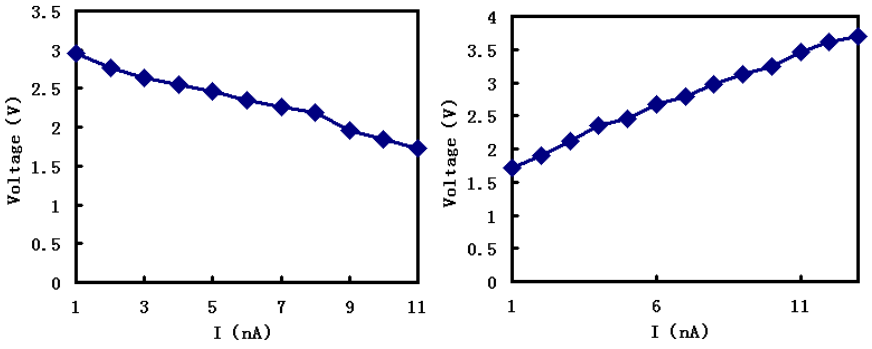


Fig.5:Simulation output results in either mode

2.5Test chip indexes

In the temperature range of -40 C~ 65 C, the measured chip indexes parameters in Table 1 below.

Table .1: Each indicator parameters of the chip

Parameter	Value
Technology	TSMC 0.35um 2P4M
Supply Voltage	5V
Input current	0.09pA～48nA
Linearity	99.3%
Integration time	20us～10ms
Voltage swing	1.3V(H-CTIA) 2V(FEDI)
Memory current error	< 1.8%
Max.clock rate	10MHz
Pixel pitch	35um×35um

Power dissipation	< 15.2mw
RMS noise	< 32uV

Conclusion

The design and implementation of a novel readout circuit mode. Through the switch circuit to meet shared amplifier, and then to control the dual purpose of pixel circuits, and in the subsequent stage sample with hold circuit and a post-amplifier circuit using an integration time adjustable thought, constructed two very good seed pixel output mode, using the principle of complementary S matrix coding regulatory thinking in the circuit to improve the read-out signal to noise ratio. The readout circuit design ideas according to the text, reduce the complexity of the circuit, increasing the flexibility of circuit applications. Through simulation and testing, the indicators to achieve preset goals, the design of the readout circuit can be used in the different sensing element, it will accelerate the speed of infrared detection technology and related fields.

Acknowledgements

The research work was supported by the National Natural Science Foundation, the grant number is: 1127437.

References

[1]GONG Hai-Mei, LIU Da-fu.Developments and trends in spaceborne infrared detectors[J].Infrared and Engineering,2008,37(1):20-23.

[2] GE JianQuan, YANG Tao, ZHANG Xiao-jin. LOS rate estimation method for strapdown imaging seeker of smart submunition[J].Tactical Missile Technology,2009(5):67-68.

[3] FAN Yang-yu, WANG Wei.Determination of IRFPA bad pixels with offset criterion[J].Infrared and Laser Engineering,2012,41(12)3173

[4] Zhou Xiao-yao,Fan Da-peng,Zhang Zhi-yong,et al.Analysis and design of multi-loop IMC controller for electroller for electro-optical serve control systems[J].Infrared and Laser Engineering,2011,40(10):2024-2026.

[5] W Lu, H J Ou, M H Chen, et al.Application of GaAs/AlGaAs multiple-quantum well infrared detector array[J].International Journal of Infrared Millimeter Waves, 1994,15:139-142.

[6] DAI Qin, SONG Wen-wu, Wang Xi-Jun.Design and stability circuit[J].Optics and Precision Engineering,2006,14(5):476.

[7] ZHANG Zhi-hai, Gao Ling-xiao,GUO Yuanjun, et al. The design and experiment of complementary S coding matrix based on digital micromirror spectrometer[J]. Spectroscopy and Spectral Analysis, 2012,32(12):3430-3431.

[8]Frehlich Rod G. Estimation of the nonlinearity of a photodetector[J].Applied Optics, 1992,31(28)5927.

[9]WU Z,CHEN X,ZHU S, et al. Room Temperature methane sensor based on grapheme nanosheets polyaniline nanocomposite thin film[J]. IEEE Sensors Jouranal,2013,13(2):777-780.

[10] YOON N, KIM B, LEE HC, et al. Highinjection efficiency readout circuit for low resistance infrareddetector[J].Letters. 1999,35(18):144.