Using reciprocity theorem to analyze R-2R network DACs

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Abstract. Reciprocity theorem is proposed to design and analyze R-2R based DAC, which can make the complicated design and analysis of R-2R based DACs simple. The detail of how to use reciprocity theorem in the design and analysis of R-2R based DAC is given. The 14-bit DAC designed by Reciprocity Theorem has performances of 69dB SNR, 11.1 bits ENOB and 77.9dB SFDR.

Introduction

R-2R network [1-3] are widely used in DAC [4-7]. Shown in figure 1 is a typical R-2R network with resistors of R lying at the bridges and resistors of 2R on the branches except for the right end with a resistor of R. From the basic circuit law, we can see the values of resistance seen from the right of nodes A, B, C, D and E——including the branch under these node——are all R. We call such feature of R-2R network to be equal-resistance feature.



If a voltage V is applied at node E, then we get V/2 at D, V/4 at C, V/8 at B, V/16 at A. That is to say, the applied voltage is scaled down. The output of an n-bit DAC can be expressed as

$$V_{out} = \sum_{i=1}^{n} b_i 2^{-i} V_{ref}$$
(1)

where b_i is a binary number which can only be 1 or 0 and V_{ref} is a reference voltage or current. From (1), we can see that the reference is scaled down and added to get the output. R-2R network and DAC have something in common, so R-2R network is widely used in building of DAC.

A simple 4-bit R-2R based DAC

Shown in figure 2 is a 4-bit R-2R based DAC. When all the switches are connected to ground except S1 is connected to V_{ref} , the resistance from the left and right of node A to ground is all 2R. So the reference V_{ref} produces voltages of $1/3V_{ref}$ at node A, $1/6V_{ref}$ at node B, $1/12V_{ref}$ at node C, and $1/24V_{ref}$ at node D. In the same way, when all the switches are connected to ground except S2 is connected to V_{ref} , the reference V_{ref} produces voltage of $1/12V_{ref}$ at node D; when all the switches are connected to ground except S3 is connected to V_{ref} , the reference V_{ref} produces voltage of $1/6V_{ref}$ at node D; when all the switches are connected to V_{ref} , the reference V_{ref} produces voltage of $1/6V_{ref}$ at node D; when all the switches are connected to V_{ref} , the reference V_{ref} produces voltage of $1/6V_{ref}$ at node D; when all the switches are connected to V_{ref} , the reference V_{ref} produces voltage of $1/6V_{ref}$ at node D; when all the switches are connected to V_{ref} , the reference V_{ref} produces voltage of $1/3V_{ref}$ at node D.



Figure 2. A 4-bit R-2R based DAC.

According to the superposition theorem, the voltage at node D is

$$V_D = \sum_{i=0}^{3} b_i \frac{1}{2^i 3} V_{ref}$$
(2)

where b_i is a binary digit which adopts 0 when the corresponding switch is open and adopts 1 when the corresponding switch is closed.

Comparing (2) to (1), we find that (2) is an expression of a 4-bit DAC. The switches in figure 2 can be controlled by digital circuit which has a 4-bit binary digital code as its input. As a result, we can input a 4-bit digital code and get corresponding analog signal level according (2).

A 5-bit R-2R DAC based on reciprocity theorem

The DAC in figure 2 or such kind of DAC requires the symmetry of the R-2R network. That is to say, the resistance from the left and right of every node on the bridge to ground must be equal, but in fact, most R-2R networks don't have such feature. Usually, only one side of practical-used R-2R networks has equal resistance on every node. Shown in figure 3 is a practical 5-bit R-2R based DAC which differs from the DAC in figure 2 in that it is un-symmetric.



Figure 3. A 5-bit R-2R based DAC.

For such architecture shown in figure 3, the equal-resistance feature of the R-2R network can't be applied directly. As we will know, using reciprocity theorem, the equal-resistance feature can also be applied. We redraw figure 3 in figure 4.



In figure 4, we use a current meter to measure the current at the output terminal. If a voltage is required at the output, Nortons theorem can be used to transformed the measured current to voltage. When only S1 is connected to V_{ref} and the rest switches are all connected to ground, figure 4 can be redrawn as figure 5.



Figure 5. Redraw of figure 4 when only S1 is connected to Vref..

In figure 5, according to the reciprocity theorem, the current meter and the voltage source can be exchanged without the changing of the measured current, as shown in figure 6. In figure 6, according to the equal-resistance feature of R-2R network, the resistance from the left of node D, C, B and A to ground are all equal to 2R—not including the 2R resistors under these nodes —so the current through the resistor between nodes D and C is $V_{ref}/(2R)$, the resistor between nodes C and B is $V_{ref}/(4R)$, the resistor between nodes B and A is $V_{ref}/(8R)$, and the current through current meter M is $V_{ref}/(16R)$. In figure 5, according to the reciprocity theorem, the current through M produced by V_{ref} is $V_{ref}/(16R)$.



Figure 6. Exchange the current meter and the voltage source in figure 5.

In the same way, in figure 4, when only S2 is connected to V_{ref} and the rest switches are all connected to ground, the current though M is $V_{ref}/(8R)$; when only S3 is connected to V_{ref} and the rest switches are all connected to ground, the current though M is $V_{ref}/(4R)$; and when only S4, S5 or S6 is connected to V_{ref} and the rest switches are all connected to ground, the current through M is $V_{ref}/(4R)$; and when only S4, S5 or S6 is connected to V_{ref} and the rest switches are all connected to ground, the current through M is $V_{ref}/(2R)$. According to the superposition theorem, the current through M is

$$I = j \frac{V_{ref}}{2R} + \sum_{i=1}^{3} b_i \frac{V_{ref}}{2^{i+1}R}$$
(3)

where b_i is a binary digit which adopts 1 when the corresponding switch is connected to V_{ref} and 0 when the corresponding switch is connected to ground; j is a decimal number which represents how many switches are connect to V_{ref} in S4, S5 and S6. Expression (3) doesn't represent a single binary-weight DAC but a combination of binary-weight and thermometer-coded DACs. We can design a digital circuit which has a 5-bit binary number as its input. The lowest 3 bits are coded to control the corresponding switches in S1, S2 and S3 in figure 3 and the highest 2 bits are first transformed to a thermometer code which is then used to control S4, S5 and S6.

Measurement

A 14-bit R-2R DAC in 0.35um process is designed by the method of reciprocity theorem. The last significant 13 bits are binary-weighted and the most significant 3 bits are fist transformed to thermometer code and then used to control the corresponding switches in the R-2R network. Shown in figure 7 are the measured performances of the proposed 14-bit DAC.



Figure 7. The measured performances of the proposed 14-bit DAC.

As shown in figure 7, the proposed 14-bit DAC has a SNR of 69dB, an ENOB of 11.1 bits and a SFDR of 77.9dB.

Conclusion

From the analysis above, we find that Reciprocity Theorem can make the complicated design and analysis of R-2R based DACs simple. The 14-bit DAC designed by Reciprocity Theorem has performances of 69dB SNR, 11.1 bits ENOB and 77.9dB SFDR.

References

- [1] D. Marche, Y. Savaria and Y. Gagnon "Laser fine-tuneable deep sub-micron CMOS 14 bit DAC", IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 8, pp.2157 -2165 2008.
- [2] V. V. B. Rao and K. S. Rao "Equivalent circuit for a multiplying D/A converter", IEEE Trans. Circuits Syst., vol. CAS-32, no. 11, pp.1199 -1200 1985.
- [3] H. Asazawa ,"D/A converter for minimizing nonlinear error", Patent 5 119 095, 1992.
- [4] M. Meunier, Y. Gagnon, Y. Savaria, A. Lacourse and M. Cadotte "A novel laser trimming technique for microelectronics", Appl. Surf. Sci., vol. 186, no. 14, pp.52 -56 2002.
- [5] R. D. Cutkosky "A new switching technique for binary resistive dividers", IEEE Trans. Instrum. Meas., vol. IM-27, pp.421 -422 1978.
- [6] Jose Bastos, Augusto M. Marques, et al. A 12-bit intrinsic accuracy high-speed CMOS DAC. IEEE J Solid-State Circuits, 1998 33(12): 1959.
- [7] A. M. Sodagar and G. R. Lahiji, "Mapping from phase to sine-amplitude in direct digital frequency synthesizers using parabolic approximation", IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 12, pp.1452 -1457 2000..