At 100mV Power Supply Accurate Ultra-Compact I-V Models for SMIC 0.18μm Process MOS Transistors with Analyses of CMOS NOT Gate and Its Amplifier

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***Abstract*—Green design features with ultra-low power consumption and ultra-low voltage supply. Considering on about 26mV is the silicon power fed limit, below 100mV level, two accurate ultra-compact I-V models for SMIC 0.18μm process N- and PMOS transistors will be extracted with which CMOS NOT gate and its amplifier are analyzed by comparing exponential power law and SPICE running tool. The modeling methodology on new device or circuit starts with a candidate for one region of features in a basic construction formulae set selected by mechanism standards, then compare the two classes of data resulted from in right side the input-output characteristic and in left side the respondings of your first to/or No.n candidate, to minimize the errors between the classes, doing in above steps in cycle, at last you met an apt of novel model group in state-of-the-art kept in your mind. In general, the ultra-low subthrethod (~25mV) MOSFETs are related to the input signals in parameters. From the single MOSFET to the two tubes we iterated from the simulation results to those models' grinded fruits in our computers, and focused on scanning the width length ratio. Our time-variant models are in form of e exponential term for NMOSFET and plus quadratic term for PMOSFET. All in all the works built up novel milestones for first author proposed brain health microelectronics (BHM).**

Keywords-ultra-low voltage; compact MOSFET models; CMOS NOT-gate; CMOS NOT-based amplifier

I. INTRODUCTION

CMOS (Complementary Metal Oxide Semiconductor) NOT was proposed by F. M. Wanlass and Chih-Tang Sah in Fairchild Semiconductor in 1963 [1~2].

Each inverter is made of a pair of PMOS and NMOS transistors under on- or off-state in turn. So far it is the basic block of digital circuits featured low power.

But into ultra-low voltage such as below 100mV power supply, there is no ready-made formulae for analyzing the MOSFETs or CMOS NOT and it's the simplist application as amplifier [3]!

Through understanding of modeling mothodology described in abstract, we will in detail assess the single MOSFET and the simplest CMOS circuits in modeling for goals of novel sensor interface design [4~9].

II. COMPACT MODEL OF NMOS

First we start with forming on formula in y=ω'*exp(β*x) by scanning parameters of NMOS based amplifier at 100mV power supply (see Fig. 1 and Table 1) [3].

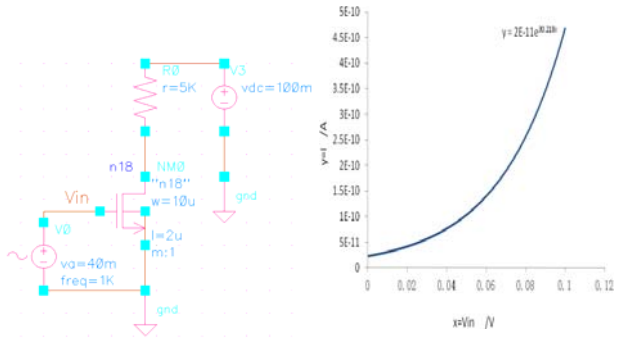

FIGURE I. (A) NMOS AMPLIFIER; (B) I-V CURVE

From left to right the I-V charateristic is depicted. Wherein x=Vin, y=Id. The key is on:

$$y = (2E-11)e^{30.22x} \tag{1}$$

TABLE I. THREE PARAMETERS' RUNNING OF FORMULA Y=Ω'*EXP(B*X) FOR NMOS

W/L / Parameters	10u/2u	100u/2u	1000u/2u	5000u/2u
ω'	2.00E-11	2.00E-10	2.00E-09	1.00E-08
β	30.22	30.22	30.22	30.22

III. COMPACT MODEL OF PMOS

In Figure 2 we care PMOS amplifier and find that this Id signal is not in sine wave, so we change the range of Vin from 0~80mV to 0~40mV.

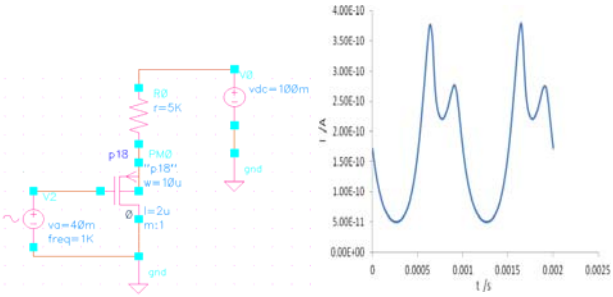

FIGURE II. (A) PMOS AMPLIFIER; (B) ID=F(T)

While we shrink the range of Vin, the interesting Id shapes can be illustrated in loop waves that every middle intecept decreased following the rise of frequence of Vin (see Figure 3~4).

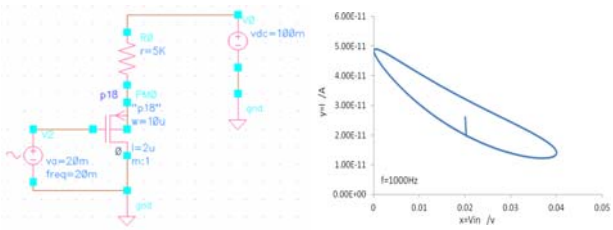

FIGURE III. (A) PMOS AMPLIFIER; (B) I-V CURVE OF 1KHZ

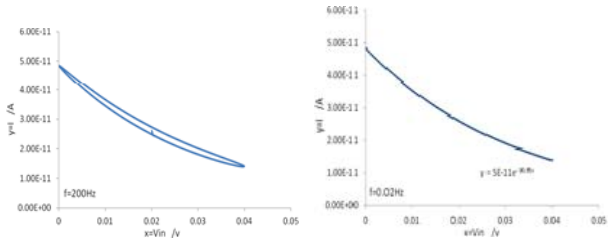

FIGURE IV. (C) I-V CURVE OF 200HZ.; (D) I-V CURVE OF 0.02HZ

Formulae (2) and (3) are based on (1) added quadratic term including decreased intecepts. Dividing output's regions we have up-branch with y1 and down-branch with y2.

$$y1=(5E-11)e^{-30.95(x-0.0.25)}+(1.5E-19)f/(x-0.015)^2 \quad (2)$$

$$y2=(5E-11)e^{-30.95(x-0.0.25)}-(1.5E-19)f/(x-0.015)^2 \quad (3)$$

Fitting Figure 4-(d) there is Table 2 showing similar relationship with Table 1.

TABLE II. THREE PARAMETERS' RUNNING OF FORMULA Y=Ω'*EXP(B*X) FOR PMOS

W/L / Parameters	10u/2u	100u/2u	1000u/2u	5000u/2u
ω'	5.00E-11	5.00E-10	5.00E-09	2.50E-08
β	-30.95	-31.07	-31.07	-31.07

IV. COMPACT MODELS VERIFICATION IN CMOS NOT GATE

In engineering glasses, a true same CMOS NOT gate (W/L=50u/0.5u) load is attacted (see Figure 5). Next we continued matching above new three models signed in formulae (1), (2) and (3).

To select three typical input frequences of 2Hz, 200Hz and 2kHz, then we compare simulated input-output wave to MATLAB 7.0 based results, verifying the validity of above matching, respectively.

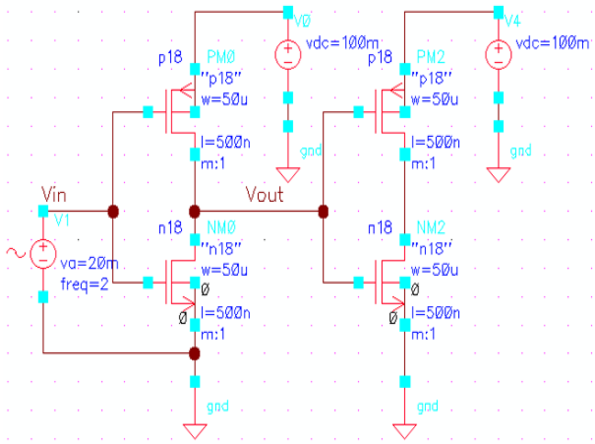

FIGURE V. CMOS NOT GATE AND ITS SAME LOAD

Simulator: spectre; T≡27C; Library: Kathy; Cell: low_inv.

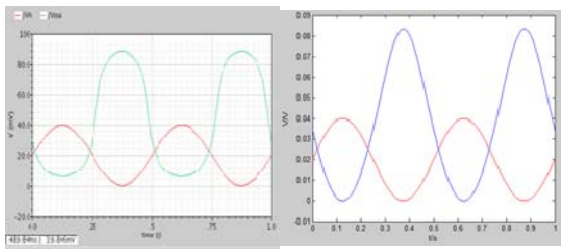

FIGURE VI. (A1) SIMULATED RESULTS @ 2HZ; (B1) MATLAB 7.0 BASED RESULTS @2HZ

Note: (1) to analyze errors has Δ amplitude of output ≤ 8.00mV;

(2) the increased branch of output has a bad negetive narrow peak in reason of discontinuous regions of computation (See sub-Fig. b2~b3).

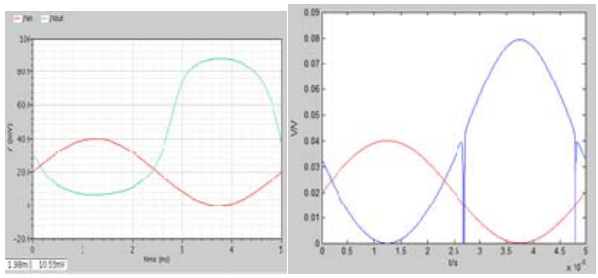

FIGURE VII. (A2) SIMULATED RESULTS @ 200HZ; (B2) MATLAB 7.0 BASED @ 200HZ

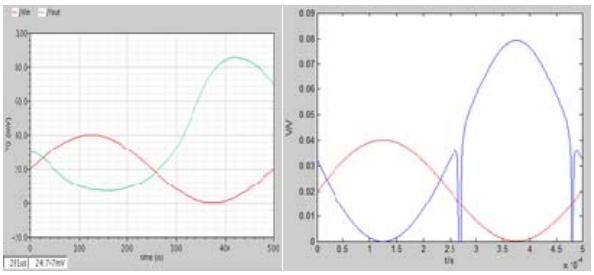

FIGURE VIII. (A3) SIMULATED RESULTS @ 2KHZ; (B3) MATLAB 7.0 BASED @ 2KHZ

V. COMPACT MODEL VERIFICATION IN CMOS NOT BASED AMPLIFIER

To add an apt biaed resisitor bringing ports Vin and Vout, so far the simplist amplifier is made (see Figure 9).

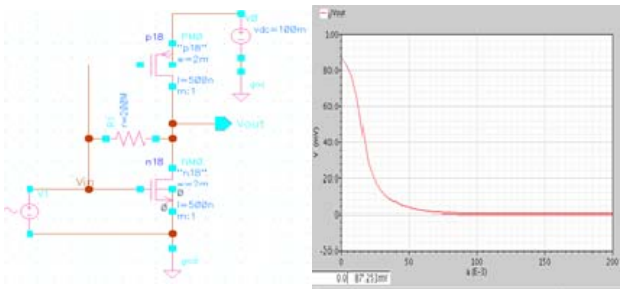

FIGURE IX. (A) CMOS NOT BASED AMPLIFIER; (B) DC SIMULATION RESULTS

Note: (1) DC Q-point = 17mV; (2) gain=13.58dB; (3) phase margin = 180; (4) This inverted amplifier is existent.

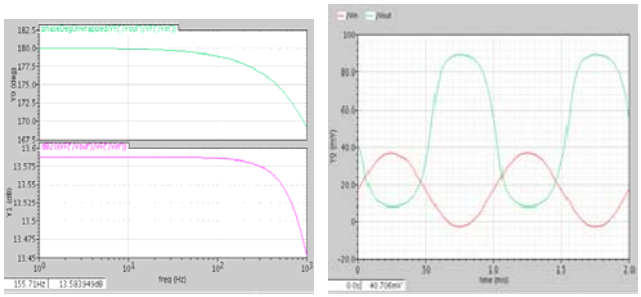

FIGURE X. (C) AC SIMULATION FROM 1HZ TO 1KHZ; (D) TRANSIENT SIMULATION RESULTS

VI. CONCLUSIONS

Supplied 100mV we model the single MOSFET and 2T-NOT gate and its amplifier with matched results.

Our model type is in form of Vout = f (f_{in},W/L, ω', β) with independent three self variables @27C. The key innovation point be on adding quadratic term for PMOSFET compared with NMOSFET model.

The future works will cover that: (1) to modify the discontinuous output wave; (2) do MPW for SMIC 018 so as to verify our models' validity furture.

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