Design of Time-to-Digital Converter for Precision Control

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***Abstract*-The time-to-digital converter is a widely used device for measuring pulse width,timing characteristic of signal in precise control. In this paper, we present a cyclic time-to-digital converter based on the pulse-shrinking technique. Through utilizing the temperature-compensated Schmitt trigger and design rules, the time resolution of pulse-shrinking cell can be precisely adjusted by controlling the high and low threshold voltage of the transition and is low temperature-dependent as well. The proposed time-to-digital converter was implemented by TSMC 0.35μm 3.3V process and the experiment results show the time resolution error of circuit is very well under the temperature range from 20°C to 100°C. In addition, within 9ns, the differential nonlinearity (DNL) and integral nonlinearity (INL) are less than ±0.1LSB and ±0.11LSB with respect to the time resolution of 47ps.**

Keywords-time-to-digital converter; pulse-shrinking; temperature-compensated; schmitt trigger; resolution error

I. INTRODUCTION

Time-to-digital converter (TDC) is widely used in precision control system [1-3]. However, the accuracy of TDC circuit may drift according to the temperature variation of the system. The temperature compensation becomes an essential design consideration to enhance the accuracy of TDC circuit. In order to enhance accuracy of analog TDCs, both accurate device sizing and careful layout methodology are proposed to achieve reducing process, voltage and temperature sensitivity [4-5].Conventional pulse-shrinking TDC allows that the pulse width under measurement is shrunk continuously by a pulse-shrinking chain.The cyclic TDCs werefurther presented to simplify calibration process [6-8].In order to stabilize time resolution of circuit, the pulse-shrinking cells used in cyclic TDCs have to be designed with low thermal sensitivity. We hence attempt to present a low thermal sensitivity cyclic time-to-digital converter based on the multi-stage pulse-shrinking technique [9] for rapidlyconverting pulse width into the corresponding digital code.

II. THE PROPOSED TDC

The proposed cyclic TDC is shown in Figure. 1 which consists of a controllogic, two pulse-shrinking delay lines, a D flip-flop chain, a digital counter and an output encoder. As shown in Figure. 1, two 3-bit pulse-shrinking delay lines, A and B, are composed of d_1~ d_8 and d_9~ d_{16}, respectively. In measurement process, the outputs (d_1~ d_8) of delay-line A are used to trigger the D flip-flop chain while the outputs (d_9~ d_{16}) of delay-line B are connected to the same D flip-flop chain as the reset signal. Then, the falling-edge-trigger counter is triggered once delay-line A and B finish shrinking both. Finally, the 8-bit Johnson code (q_1~ q_8) is produced by the D flip-flop chain and then encoded into a corresponding 4-bit binary code. According to the method mentioned above, the measured time interval W_{meas} can be calculated finally.

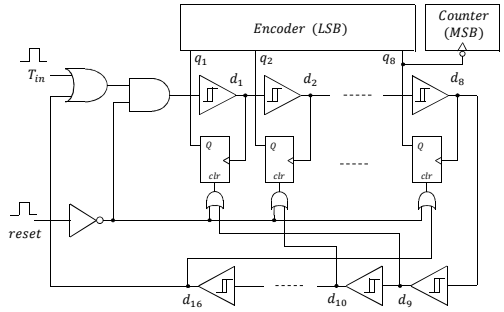

FIGURE 1. THE PROPOSED CYCLIC TIME-TO-DIGITAL CONVERTER.

III. THE PROPOSED PULSE-SHRINKING CELL

Providing a stable time resolution of pulse-shrinking against temperature changes is one of important goals for designing a cyclic TDC. For this reason, the temperature characteristic of the high and low threshold voltages of Schmitt inverter is employedas the fundamental concept of designing a pulse-shrinking cell with temperature compensation. Figure. 2shows a conventional Schmitt trigger which consists of a Schmitt inverter and a CMOS inverter.

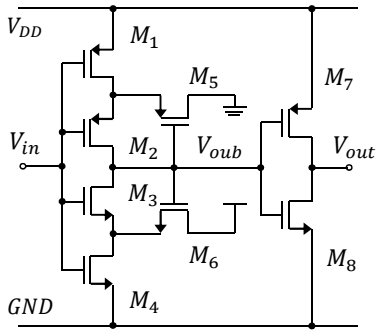

FIGURE 2. THE CONVENTIONAL SCHMITT TRIGGER.

The pulse-width difference between the input and output signal of the Schmitt inverter is highly related to temperature variation and can be expressed as:

$$W_d = \left[\frac{W_{r_{in}}(T)+W_{f_{out}}(T)}{0.8V_{DD}}\right]\cdot\left[V_{th_H}(T)-S\right]-\left[\frac{W_{f_{in}}(T)+W_{r_{out}}(T)}{0.8V_{DD}}\right]\cdot \left[S-V_{th_L}(T)\right], \quad (1)$$

whereT is the absolute temperature in degrees Kelvin and S is half of supply voltage.In order to improve the time resolution of pulse-shrinking against the influence of temperature variation, the exact condition for obtaining the desired time resolution of pulse-shrinking and minimizing the error caused by temperature has to be derived clearly. Unfortunately, the rise and fall times are not only a function of temperature but also of the high and low threshold voltages. That means that the transistors with different size ratio will not only define the different high and low threshold voltages, but also change the rise and fall times and the quantity of pulse-shrinking. The relationship between temperature and quantity of pulse-shrinking appears to be a complex parabolic curve. Therefore, based on Schmitt inverter circuit, it is too difficult to derive an exact condition for designing a pulse-shrinking cell with temperature compensation unless the rise and fall times are assumed to be temperature independent. We hence attempt to derive an approximate condition as a basis for minimizing the pulse-shrinking error caused by temperature variation. For convenience of analysis, the rise and fall times are assumed to be temperature independent and constant.If we assume that the PMOS/NMOS transistors are with the same process parameters, the temperature dependence of both high and low threshold voltages would only depend on threshold voltages of the NMOS and the PMOS transistor respectively.By calculating $\partial W_d/\partial T = 0$, the approximate condition for minimizing the pulse-shrinking error caused by temperature can hence be derived and expressed as:

$$\frac{-\sqrt{\frac{\beta_4}{\beta_6}}}{1+\sqrt{\frac{\beta_4}{\beta_6}}} = 2\frac{-\sqrt{\frac{\beta_1}{\beta_5}}}{1+\sqrt{\frac{\beta_1}{\beta_5}}}, \quad (2)$$

where $\beta_i = \mu_o C_{ox}(W/L)$ and the temperature coefficient of threshold voltage ofPMOS transistor is twice larger than that of NMOS transistor in the TSMC 0.35μm 3.3V CMOS process.According to the equation above, for obtaining the minimum thermal sensitivity, the size ratios of transistors have to be designed to satisfy the conditions$\beta_4 \ll \beta_6$ and $\beta_1 \ll \beta_5$ or $\beta_4 \gg \beta_6$and $\beta_1 = \beta_5$.However, the strange sizing strategy on transistors is unfortunately out of expectation. It is difficult to approximate the condition by sizing transistors with reasonable size ratio. We therefore modify the conventional Schmitt trigger as shown in Figure. 3.

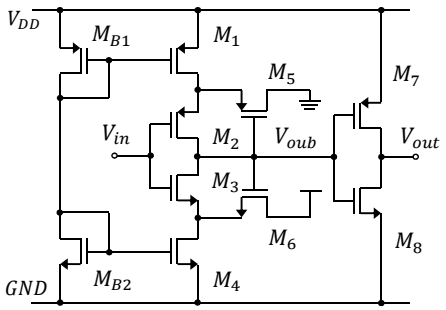

FIGURE 3. THE PROPOSED SCHMITT TRIGGER.

The Schmitt inverter is biased by a simple self-biased voltage reference. The high and low threshold voltages of proposed modified Schmitt inverter can be respectively expressed as:

$$V_{th_H} = V_{DD} - \frac{\sqrt{\frac{\beta_4}{\beta_6}}\times\sqrt{\frac{\beta_{B1}}{\beta_{B2}}}}{1+\sqrt{\frac{\beta_{B1}}{\beta_{B2}}}}\times\left(V_{DD}-V_{tp}-V_{tn}\right), \quad (3)$$

$$V_{th_L} = \frac{\sqrt{\frac{\beta_1}{\beta_5}}}{1+\sqrt{\frac{\beta_{B1}}{\beta_{B2}}}}\times\left(V_{DD}-V_{tp}-V_{tn}\right) \quad (4)$$

The temperature dependence of both high and low threshold voltages are mainly depended on the threshold voltage of both PMOS and NMOS transistors. Because the denominators are fixed, their gain can be easily controlled by tuning the size ratio of transistors β_4/β_6 and β_1/β_5. It is beneficial to approximately minimize the pulse-shrinking error cause by temperature variation. In practice, although the error can be minimized approximately, the relationship between error and temperature still appears to be parabolic curve because the rise and fall times of signal are temperature dependent. That is, the output pulse width of proposed Schmitt inverter decreases parabolically with respect to temperature. In general, the threshold voltage of CMOS inverter, V_{sp}, is temperature dependent which increases parabolically with increasing temperature. The pulse-width of the shrunk input pulse signal after passing the CMOS inverter will be enlarged with few picoseconds. That is, although the quantity of pulse-shrinking of proposed Schmitt inverter decreases parabolically with respect to temperature, it can be compensated to be almost temperature independent after passing the CMOS inverter.

IV. EXPERIMENTAL RESULTS

In this section, we demonstrate the practicability of proposed Johnson code cyclic TDC through implementing the circuits of Figure. 1 and Figure. 3 in TSMC 0.35μm 3.3V CMOS process. The experiment results of proposed cyclic TDC are reported in Figure. 4showing the time resolution of modified Schmitt-trigger-based pulse-shrinking cell compared to that of conventional Schmitt-trigger-based pulse-shrinking cell.Within the range of $25^oC$to 100^oC, the maximum error of pulse-shrinking is merely 1.3ps which is much less than that of the pulse-shrinking cell without temperature compensation. The maximum difference in converted binary code is merely 3 codes within the range of 0.5ns to 9.5ns at different case of temperatures. Moreover, the estimated DNL and INL are within ±0.1LSB and ±0.11LSB.

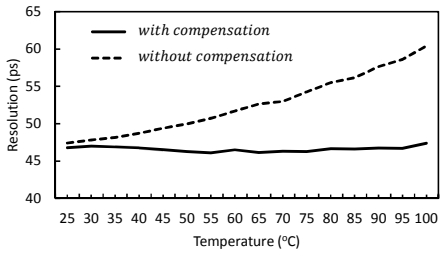

FIGURE 4. THE TIME RESOLUTION OF SCHMITT-TRIGGER-BASED PULSE-SHRINKING CELL WITH RESPECT TO TEMPERATURE.

V. CONCLUSION

In this paper, we have presented a low thermal sensitivity cyclic time-to-digital converter based on the pulse-shrinking technique.To deal with temperature dependence of time resolution of Schmitt-trigger-based pulse-shrinking cell, we bias the conventional Schmitt trigger with a simple self-biased voltage reference to flexibly control the high and low threshold voltage of the transition for minimizing the time resolution error of pulse-shrinking. In addition, based on the multi-stage pulse-shrinking technique, the proposed cyclic time-to-digital converter can be applied to rapidly convert long pulse width into the corresponding digital code. The simulation results show that the time resolution error of proposed design is 1.3ps and the estimated DNL and INL are ±0.1LSB and ±0.11LSB with respect to the time resolution of 47ps under the implement of TSMC 0.35μm CMOS process with 3.3V power supply.

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