Low Noise CMOS Transconductance Amplifier for GPS Applications

P. Katolkar
Department of Electronics Engineering
Shri Ramdeobaba College of Engineering & Management
Nagpur 440013, India

D. Dahigaonkar
Department of Electronics Engineering
Shri Ramdeobaba College of Engineering & Management
Nagpur 440013, India

D.G. Wakde
P. R. Patil College of Engineering & Technology
Amravati, India

***Abstract*—In recent years, due to distinct advantages of CMOS, the research emphasis is on use of CMOS technology rather than bipolar or BiCMOS at Radio Frequency applications. One such example is Transconductance Amplifiers used in various Global Positioning System (GPS) applications. This paper describes a CMOS Operational Transconductance Amplifier (OTA) intended for use in front-end of Global Positioning System (GPS) receiver. The proposed CMOS OTA is a three stage amplifier with fully integrated direct conversion architecture without surface acoustic wave (SAW) filter, implemented in 180nm standard TSMC process technology. The simulation results indicate high power gain of the order of 20.63 dB with noise figure of 4.7 dB & the third-order input referred intercept point (IIP3) is found to be 7 dBm. The proposed amplifier has high linearity, low noise figure with transconductance of 121mS that makes it suitable for use in GPS systems.**

Keywords-CMOS OTA; GPS; receiver; transconductance amplifier; active feedback; sdc

I. INTRODUCTION

There is large enthusiasm in the consumer market to explore capabilities of Global Positioning System (GPS). Manufacturers of cellular telephones, portable computers, and other mobile devices are looking for ways to incorporate GPS into their products. For many of these hand-held devices, one of the primary concerns is battery life. Thus, there is strong motivation to provide better system performance at very low power. This in-turn demands for optimized CMOS amplifier that has high performance with very low power consumption.

CMOS OTA is a first building block, after antenna, in GPS receivers which is specially designed to detect a low power signals. At such a low power, the amplifier must have extremely low noise & high linearity. Thus, it is necessary that the CMOS amplifier should have large gain to suppress noise from the subsequent stages with minimum harmonic distortion.

II. ABOUT GLOBAL POSITIONING SYSTEM

Presently, GPS is fully operational and meets the criteria established in the 1960s for an optimum positioning system. This system provides accurate, worldwide, continuous, three-dimensional position and velocity information to users with the appropriate receiving equipment. GPS can provide service to an unlimited number of users since the user receivers operate passively (i.e., receive only) [1]. The satellites broadcast ranging codes and navigation data on two frequencies using a technique called code division multiple access (CDMA) [1].

All GPS satellites broadcast at the two frequencies, 1.57542 GHz (L1) and 1.2276 GHz (L2). [2,3]L1 carrier is modulated by both the P and C/A codes [1], while the L2 carrier is only modulated by P (Y) code [4]. The L3 signal at a frequency of 1.38105 GHz is specially used to transmit the data from the satellites to ground stations, and this data is used by the United States Nuclear Detonation (NUDET) Detection System (USNDS) to detect, locate, and report nuclear detonations (NUDETs) in the Earth's atmosphere and near space. [5] The L4 band at 1.379913 GHz is being studied for additional ionospheric correction. [2] The L5 frequency band at 1.17645 GHz was included in the process of GPS modernization. L5 is also used by Indian navigation system IRNSS. L5, the third civil GPS signal, will eventually support safety-of-life applications for aviation and provide improved availability and accuracy [6].

III. PROPOSED CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Figure 1 indicates proposed CMOS OTA having high gain and low noise figure. The circuit comprises of three stages, trans-conductance stage, feedback stage, and single to dual convertor stage.

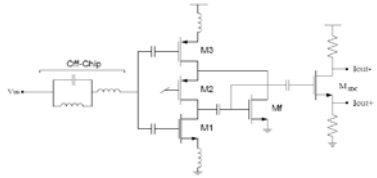

FIGURE I. THE PROPOSED CMOS OTA.

A. About Operational Transconductance Amplifier

The transconductance amplifier converts input voltage in to the current at output. The equation for output current is

$$g_m . v_{in} = i_{out} \tag{1}$$

Where gm is transconductance of an amplifier. The output current iout is conveyed to the load impedance. In conventional low noise amplifiers, linearity is limited by gm*ro where ro is output impedance. As a result, low noise amplifiers require high power to achieve linearity. In order to obtain expression for output current of OTA, we consider the basic equations of output current & gm as

$$I_{D_{n,p}} = \frac{1}{2}\mu_{n,p} C_{ox} \frac{W}{L}(|V_{GS}| - |V_{th}|)^2 [1 + \lambda(V_{DS} - V_{eff})] \tag{2}$$

$$g_m = \left(\frac{\partial I_d}{\partial V_{GS}}\right)_{V_{DS,const.}} = \mu_{n,p} C_{ox} \frac{W}{L}(|V_{GS}| - |V_{th}|)[1 + \lambda(V_{DS} - V_{eff})] \tag{3}$$

A MOSFET is operated in the saturation region since the highest linear amplification can be achieved in this region. Operating a MOSFET in saturation region produces a current in response to its gate-source overdrive voltage. A figure of merit can define how well a device converts a voltage to a current. The figure of merit is defined for the change in the drain current divided by the change in the gate-source voltage and it is called transconductance.

B. The Transconductance Stage

Figure 2 shows the transconductance stage for CMOS OTA, M1& M3 NMOS-PMOS pair forms a CMOS which is responsible for improved transconductance. A cascode cell can be used for both the NMOS and PMOS transistors.

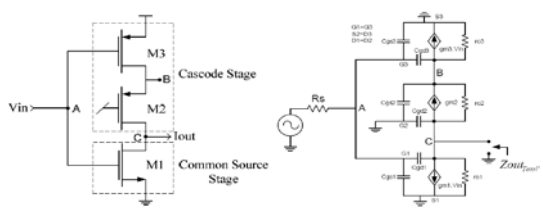

FIGURE II. TRANSCONDUCTANCE STAGE & ITS SIMPLIFIED AC MODEL.

However, cascoding both the NMOS and PMOS devices will increase the minimum noise figure of the transconductance stage, hence cascoding one of the input transistors is preferable from noise considerations. In this design, the input PMOS transistor is chosen to be cascoded, because, when biased at the same drain current, PMOS transistor will be approximately three times bigger than NMOS for equal drain-source voltage. While cascoding improves the bandwidth and the reverse isolation of the amplifier, it has some drawbacks such as contributing noise to the circuit and reducing the headroom of each transistor. The voltage transfer function of the circuit shown in Figure 2 is given by

$$A_{V_{GmAmplifier}}(jw) = \frac{v_c}{v_{in}} = \frac{-(g_{m_3} + g_{m1}) r_{O_1}}{(1 + jwC_A R_s)(1 + jwC_c r_{O_1})} \tag{4}$$

C. Active Feedback Stage

In order to improve the overall linearity of the CMOS OTA, a shunt negative feedback is proposed which utilizes an active device. The corresponding negative feedback is performed via Mf which is connected as shown in Figure 3 Mf is a feedback transistor and M2 is a current buffer that isolates Mf from node X. Therefore, the voltage at node X is multiplied by gmf and the generated current is subtracted from the current generated by M1 and M3.Eq. 5 express the IIP3 of the circuit shown in Figure 3. It can be said that the first order and third order terms are summed at the output.

$$IIP3 = \sqrt{8\left|\frac{g_{m1} + g_{m3}}{\ddot{g}_{m1} + \ddot{g}_{m3}}\right|} \tag{5}$$

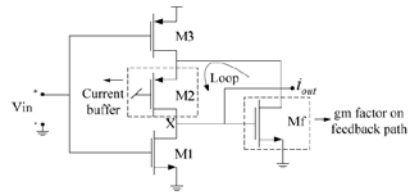

FIGURE III. ACTIVE FEEDBACK STAGE.

D. Inductive Source Degeneration for Transconductance Stage

Inductive source degeneration is introduced in order to achieve simultaneous power and noise matching [7]. Similar approach can be seen in [8], [9], and [10]. This source inductors result in higher input impedance, the input stage is comprised by NMOS and PMOS transistors which are degenerated by the inductors. Result in reduction in NF.

E. Common Drain/Source Single Ended to Differential Converter

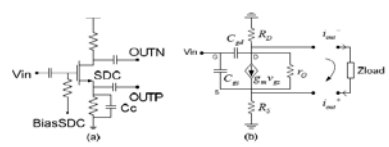

FIGURE IV. SDC CONVERTER & ITS SMALL SIGNAL MODEL.

Figure 4 shows the schematic of the phase splitter which provides differential signals of equal amplitude [11]. At high frequency, this circuit is limited by the imbalances caused by the parasitic capacitances of MOSFET. However, the phase error can be compensated by connecting a capacitor between the source node of M1 and ground [12]. Each output port is loaded by one-half of the differential load impedance & mathematically expressed as

$$Z_{DrainLoad} = Z_{SourceLoad} = \frac{Z_{Load}}{2} = R_L \tag{6}$$

Differential output single input transconductance of the SDC is expressed by

$$g_{mSDC} = \frac{i_{out+} - i_{out-}}{v_{in}} \tag{7}$$

IV. Experimental Results and Simulations

The S-parameters simulation results for the CMOS OTA are depicted in Figure 5 for GPS band-L1 to L5.Forward Power Gain of proposed CMOS OTA is found to be ranging from 10.58 dB to 20.63 dB over the GPS L-bands. The input return loss is of the order of -6.87 dB to -14.28 dB over the GPS L-bands. The simulation result indicates excellent reverse isolation ranging from -43.58 dB to -57.35 dB over the GPS L-bands.

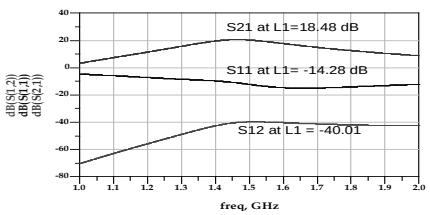

FIGURE V. S-PARAMETERS FOR BAND L1.

Figure 6 indicates that the designed OTA has comparatively less noise figure ranging from 4.7 dB to 6.2 dB over the GPS L bands, which is advantageous for its use in GPS receivers. The Simulation result indicates IIP3 of 7 dBm, resulting in reduction in nonlinearities due to intermodulation distortion.

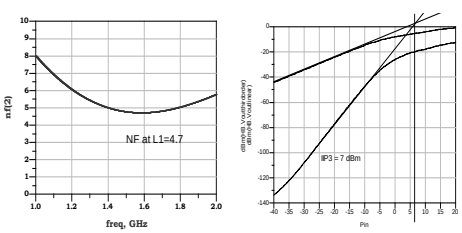

FIGURE VI. NOISE FIGURE AND IIP3.

TABLE I .COMPARISON WITH PREVIOUS WORK FOR GPS BAND L1.

Parameters	This Work	[13]	[14]	[15]	[16]
Frequency (GHz)	1.57	1.57	1.57	1.57	0.8-6.2
Technology(µm)	0.18	0.18	0.18	0.18	0.13
Power Supply(Volts)	1.8	0.7	1.8	1.8	1.5
Power Gain (S21) (dB)	18.48	17	14	18.75	25.1
Input Return Loss (S11)(dB)	-14.28	-8	-10	-10.4	-17
Reverse isolation(S12) (dB)	-40.01	-	-	-	-
Noise figure(dB)	4.7	4.2	3.2	2.52	5.73
IIP3 (dBm)	7	-14	-	-19.7	0.9
1 dB Compression Point (dBm)	-8	-	-6.35	-29.2	-
Power Consumption (mW)	29	1	30	1.93	35

V. Discussion of Results

The comparative analysis in Table I shows that the designed OTA has improved power gain of the order of 18.48 dB at 1.57 GHz frequency. The input Return loss is found to be -14.28 that indicate better input matching. Although, there is improvement in parameters like gain, input matching, linearity, IIP3 etc. the noise figure is slightly more. The use of resistors and more number of transistors contributes in noise figure, but trade off have to be made in designing the practical OTA circuits. Also, the power consumption is low, of the order of 29mW, as compared to the components used in the design. The IIP3 is found to be 7dBm that indicates improved linearity of the output signal. Thus, the proposed amplifier design presents a suitable balance between linearity, power consumption and noise figure which makes it suitable for use in wide ranging GPS applications.

References

[1] Misra, Pratap; Enge, Per (2006). Global Positioning System. Signals, Measurements and Performance (2nd ed.). Ganga-Jamuna Press. p. 115. ISBN 0-9709544-1-7.

[2] Global Positioning System, www.wikipedia.com

[3] Kaplan, Elliott D., and Christopher J. Hegarty, eds. Understanding GPS: principles and applications. Artech house, 2005.

[4] Borre, Kai; M. Akos, Dennis; Bertelsen, Nicolaj; Rinder, Peter; Jensen, Søren Holdt (2007). A Software-Defined GPS and Galileo Receiver. A single-Frequency Approach. Springer. p. 18. ISBN 0-8176-4390-7.

[5] Text Generator Version 2.0. "United States Nuclear Detonation Detection System (USNDS)". Fas.org. Retrieved November 6, 2011.

[6] "Air Force Successfully Transmits an L5 Signal From GPS IIR-20(M) Satellite". LA AFB News Release.

[7] Gatta F. et al., “A 2-dB noise figure 900-MHz differential CMOS LNA,” Solid-State Circuits, IEEE Journal of, vol.36, no.10, pp.1444-1452, Oct 2001

[8] Jung-Suk Goo et al., “A noise optimization technique for integrated low-noise amplifier”, Solid-State Circuits, IEEE Journal of, vol. 37, no. 8, August 2002.

[9] Trung-Kien Nguyen et al., “CMOS low noise amplifier design optimization techniques”, The 47th IEEE International Midwest Symposium on Circuits and System.

[10] Leonid Belostotski et al., “Two-port noise figure optimization of source-degenerated cascode CMOS LNAs”, Analog Integrated Circuits and Signal Processing, vol.55, no.2,May, 2008

[11] Marc E. Goldfarb et al. “A Novel MMIC Bi-phase Modulator with Variable Gain Using Enhancement-Mode FETs Suitable for 3V Wireless Applications”, Microwave and Millimetre-Wave Monolithic Circuit Symposium, IEEE, 1994.

[12] J. Ryynanen et al., "A dual-band RF front-end for WCDMA and GSM applications, "Solid-State Circuits, IEEE Journal of , vol.36, no.8, pp.1198-1204, Aug 2001

[13] Wenbo Xia; Xiaolin Zhang, "A low power low noise amplifier for portable GPS receivers," Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on , vol., no., pp.793,796, 23-25 July 2009

[14] Jing Shen; Xiaolin Zhang; Wenbo Xia, "A Wideband CMOS Low-Noise Amplifier for Dual-Band GPS Receiver," Wireless Communications Networking and Mobile Computing (WiCOM), 2010 6th International Conference on , vol., no., pp.1,4, 23-25 Sept. 2010.

[15] Tang Tang; Tingting Mo; Dongpo Chen, "A low-noise amplifier using sub threshold operation for GPS-L1 RF receiver," Electrical and Control Engineering (ICECE), 2011 International Conference on , vol., no., pp.4257,4260, 16-18 Sept. 2011.

[16] Kim, Ju Sung (2011). Broadband RF Front-End Design for Multi-Standard Receiver with High-Linearity and Low-Noise Techniques. Doctoral dissertation, Texas A&M University.