Study STATCOM with Small Time-Step Simulation on FPGAs

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***Abstract*—STATCOMs are installed in Power grids all over the world with its powerful reactive power support and other various functions. The STATCOM simulation technology is also promoting greatly. FPGAs, as a newly processor, are considered in STATCOM simulation to realize the small time-step, which could increase precision greatly. This paper deeply studies FPGA implementation in STATCOM simulation. Firstly, the modelling of STATCOM on FPGA is briefly studied. The modelling includes electric topology and control schemes. Then, the realization of FPGA simulation demonstrates the structure of this FPGAs simulator. Finally, the paper will carry on multiple tests and comparison to show the validation and advantage of STATCOM simulation with small time-step on FPGAs.**

Keywords-FPGA; small time-step; STATCOM; simulation; modelling

I. INTRODUCTION

STATCOMs belong to a type of FACTS (Flexible AC Transmission Devices), which can provide reactive power without being affected by disturbances coming from the AC system where they are installed. STATCOMs have been generally replacing SVC and other FACTS, as a preferred kind of reactive compensators.

Along with the development of STATCOM, the requirement on the analysis and simulation of STATCOM increases as well. The traditional simulation of STATCOM can use PSCAD/EMTDC, an offline simulation tool, which could run on a small time-step (1-2μs) to ensure precision. However, such is the compromise, that the smaller time-step implemented induces longer calculation time. Whatever the offline simulation could ignore the time-consumption, the real-time simulation has to be realized with very high simulation efficiency[1].

Small time-step is now a challenge for real-time simulations. Currently, famous RT-LAB can only recommend 20μs for STATCOM simulation in its server platform. RTDS can provide a small time-step simulation for STATCOM, but the scale of circuits is limited seriously[2]. It is cause by a simple reason that traditional simulators rely on CPUs and Operation systems, which will account for a great part of time in each small time-step.

FPGA, (Field — Programmable Gate Array), is an integrated circuit designed to be configured by a customer or a designer after manufacturing. Historically, FPGAs have been slower and generally achieved less functionality. However, contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations[3].

FPGAs have been considered in power system simulations several years ago [4]. The outstanding feature of modern FPGAs on simulations is their reconfiguration and parallel computation capability, as well as the fast I/O and bidirectional data buses [5]. Earlier applications are an independent VSC (Voltage Source Converter) simulation in hardware testing. FPGAs provide fast I/Os and small time-step computation in these cases. However, only fixed topology for VSCs with limited circuit elements, due to limited resources on FPGAs, are too inconvenience to be implemented widely[6]. When a new generation of FPGAs is applied, circuits that are more complex can be simulated on FPGAs. People dismayed again, however, when they wished that the simulation on FPGAs can be used for analysis and evaluation, not only for testing the hardware. This generation cannot support double float point computation to increase precision because of limitation of resources as well.[7].

When most recent FPGAs, such as Xilinx Virtex-7, come out, they provide several times of resources and higher performances. This promotion supports that tcircuits simulation, such as STATCOMs and VSC-HVDCs, with larger scale and more precision can be achieved.

This paper studies how to explore the simulation of STATCOM in the new generation of FPGAs. The features of this simulator are both double float point computations and flexible modellings. In the next section, the modelling of STATCOM is deeply studied on FPGAs, This modelling is based on discrete elements instead of a fixed topology. Then, the configuration of hardware of a FPGAs simulator is demonstrated briefly. Finally, the case study is illustrated to verify precision and efficiency with analyses and comparison of STATCOM in disturbances.

II. STATCOM MODELLING ON FPGAS

The simulator on FPGAs utilized in this paper, is specially designed to model circuits with discrete elements. This simulator ensures the variety in modelling and supports flexible simulation.

The modelling of STATCOM is various. The basic mathematic function modelling that has widely implemented is not flexible due to its fixed topology. This paper studies the modelling with discrete elements, which is just supported by supposed FPGA simulators.

Besides, topologies of STATCOM in pratical terms vary from two levels, three levels to chain links. This paper discusses the modelling of two levels, but the modelling of other topologies is similar with discrete elements.

A. *Circuits Topology*

This paper builds the model of STATCOM, as shown in Figure.1.

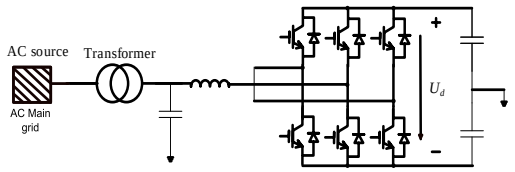

FIGURE I. .CIRCUITS TOPOLOGY OF STATCOM.

STATCOM consists of three main components in AC sides, An AC voltage source with an internal reactance, a transformer and a LC resonant filter.

Normally, two level converters, converters of chain links, three level converters or double converters, transfer AC to DC. Two level convertersarestudied in this paper for the simple reason that it is simple to verify the feasibility of FPGA simulators with small time-step. This converter is modelled with discrete circuits, includes IGBTs (Insulated Gate Bipolar Transistor), diodes, snubber circuits (series capacitor and resistor branches) and voltage and current meters.

Two large DC capacitors connect to the ground and balance DC voltage on two poles.

The detailed parameters of the circuits are shown in table 1.

TABLE I .THE PARAMETER OF THE DC GRID.

DC sides		**AC sides**		**Converter Parameter**	
C1	100[μF]	Xs	12.7[mH]	Vfwd	0.01[kV]
C2	100[μF]	Rs	0.1[Ω]	Ileak	0.00001[kA]
		XT	12.7[mH]		
fswitching	2000[Hz]	RT	2[Ω]		
RL	2[Ω]	L	15.9[mH]		
LL	88[mH]	Pave	70[MW]		
		Es(L-L)	90[kV]		

B. *Controller Modelling*

The controller of STATCOM is illustrated in Figure. 2.

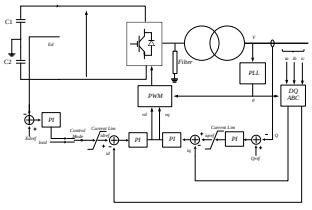

FIGURE II. CONTROL SCHEME OF STATCO.

The controller is the typical double loop control scheme, which consists of an inner loop and outer loop. The outer loop has also two regulations, a reactive power regulation accessing the reference of inner reactive power regulation and an active power regulation accessing the reference of inner active power regulation. These two regulations can select the different control target in the different modes. The active power regulation always controls the voltage in capacitors, C1 and C2. Besides, the active power through the converter is selected as the reference in an emergency. The reactive power regulation can switch freely and instantaneously between the reactive control and the AC voltage control. The inner loop includes an active power current regulation and a reactive power current regulation with upper and lower limit. The parameters of PIs are adjusted deliberately to obtain a fast tracking response.

III. CONFIGURATION OF A SIMULATOR ON FPGAS

The simulator on FPGAs is special designed for flexible modelling and simulation. The configuration and outward viewing is illustrated in Figure.3.

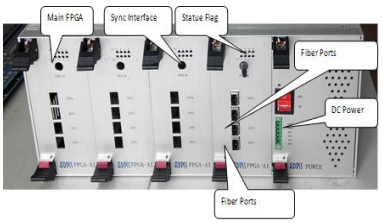

FIGURE III. THE APPEARANCE OF THE SIMULATOR.

In the figure above, there are tags on the different parts of this simulator. “Main FPGAs” represents a board of a computation core, which is built on Virtex-7 FPGA. This core is responsible for the data processing and network integration. The computation ability of this board determines the simulation ability. In this time, each “Main FPGA” card can support the simulation with a network containing more than 60 buses, 200 resistors or inductors, 20 single-phase transformers, 20 power sources and other crucial elements in power system simulation.

“Sync Interface” is a synchronization channel with IRIG-B code, which provides the synchronization with the microsecond level precision.

The panel of “Statue Flag” can show eight different statues with different LEDs. It has eight statues of “Power on or not, Programming or not, Running or not, Halting or not, Synchronizing or not, I/O working or not, Data communication or not” and one for reserving”.

Besides, this simulator provides can extend the simulation scale with four fiber channels. Also, these channels can be used independently, such as the external I/O, the communication with other boards, the communication with local server and the interface for practical controller.

“DC Power”, which is a ±12V DC supply, cannot be neglect in this simulator.

IV. CASE STUDY OF STATCOM

This paper carried on STATCOM testing on the simulator on FPGAs deliberately. Firstly, the results have to be compared between FPGA simulator and PSCAD, a feasible Electromagnetic simulation tools. This can verify the precsion of FPGA simulator. Then, this paper will utilize this platform and STATCOM models to carry on various tests. To be complete, tests will cover all the operation conditions, including steady states and disturbances.

A. *Steady States Precision Verification*

In this part, not only has a scope been used to sample the circuit electric quantities, such as voltages and currents, while simulation results will be stored in memory on FPGAs, which can be read later. The results in the scope are shown on Figure. 4.

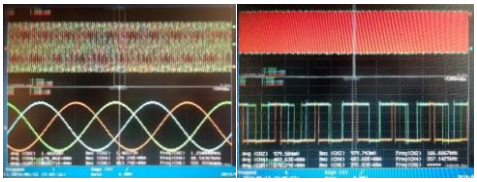

FIGURE IV. VOLTAGES ON AC SYSTEM AND THE OUTPUT OF STATCOM IN THE SCOPE.

The previous figure represents voltages of AC system and outputs of the converter in STATCOM. Also this paper extracts a short waveform of on the simulator, comparing with the results in PSCAD, as shown in Figure. 5.

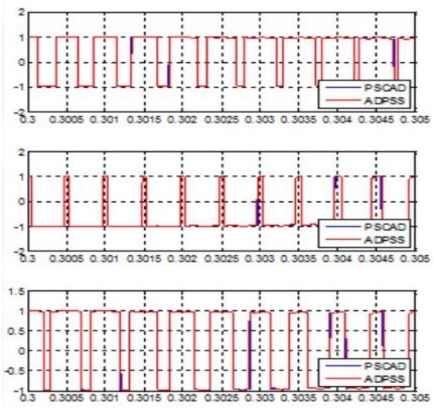

FIGURE V. COMPARISON OF PSCAD AND FPGAS(ADPSS).

From Figure. 5, the red line, which represents output on simulator on FPGAs, is wholly coincide with the blue line, which is the results of PSCAD. This comparison shows the validation of simulator output.

B. *Response in Disturbances*

On the simulator of FPGAs, this part shows the response of STATCOM in disturbances, a DC disturbance and an AC disturbance.

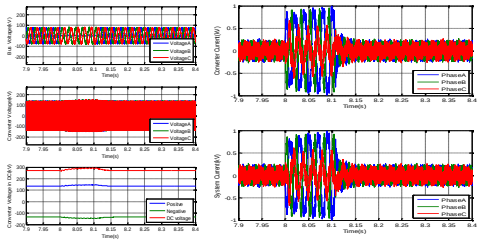

FIGURE VI. VOLTAGES AND CURRENTS FOR AC DISTURBANCES.

The AC fault happens at 8 s, and lasts 0.1 s. As shown in Figure. 6, bus voltages for AC system greatly drop down in Phase A. Voltages at the output of the STATCOM, however, decrease much more slightly due to supports from the STATCOM. DC voltages in DC sides of STATCOM rises slightly, and returns to the normal operation condition rapidly when the disturbance is cleared. Currents from STATCOM, as shown in Figure. 8 increased, which are equivalent to the current injected to AC systems.

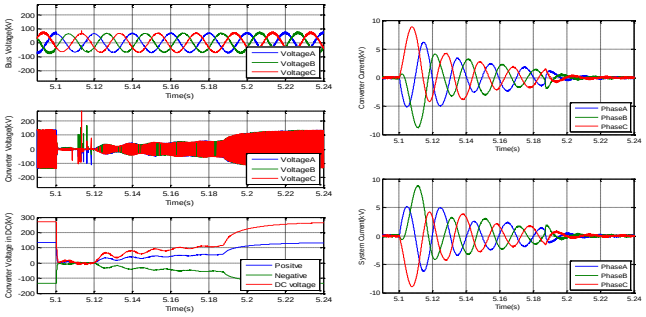

FIGURE VII. VOLTAGES AND CURRENTS FOR DC DISTURBANCE

The responses of STATCOM in DC disturbance are entirely different, as shown in Figure. 7. The fault begins at 5.1s. The DC voltage of STATCOM immediately has been flying into near the ground. The injected currents increase to a dramatically large value. At 5.12s, the fault is clear and STATCOM begins to recover the normal operation. Then, STATCOM enters the normal state after 70ms.

These results show that STATCOM on the simulator of FPGAs can obtain the reasonable response in various disturbances.

V. CONCLUSION

This paper studies how to model a STATCOM with a small time-step on FPGAs. The modelling of STATCOM with discrete elements is proposed. The main topology is discussed, and the converter and other element are deliberately selected to coincide with the requirement of testing on FPGAs.

Besides, the control system, which builds on the FPGA simulator as well, includes double loops control and mode selections. This control scheme can be implemented in lots of fields to provide rapid and steady control capability.

The structure of FPGA platform has been illustrated, including the FPGA cards and interfaces. Each FPGA cards can provide strong simulation capability. In addition, the simulator can enhance its simulation capability with extending FPGA cards. It shows that this FPGA simulator can meet various test conditionsand requirements.

A STATCOM built on this simulator with a small time-step. The performance in normal operations and in disturbances shows the validation of the modelling of STATCOM on FPGAs. Hence, this modelling and simulation can applied in more fields later.

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