A 1.9 GHZ High Efficiency Class-F SOI CMOS Power Amplifier

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***Abstract*—In this paper, a 1.9 GHz high efficiency power amplifier (PA) for wireless applications is present. The PA is a two stage class-F power amplifier. The drive stage is self-biased cascode structure and the output stage is common source. The PA is designed and simulated in 0.18 μm silicon-on-insulator (SOI) technology. The simulation results show that at 1.9 GHz, this class-F PA can achieve 50 % PAE (power added efficiency) at (1dB compression point) output power of 25 dBm and the linear gain is 20 dB.**

Keywords-power amplifier; class F;SOI; efficiency

I. INTRODUCTION

Nowadays the wireless communication systems are in a rapid development. Cell phones, WLAN (wireless local area network) modems, laptops are everywhere. All of these systems require transmitting signals efficiently to save battery lifetime. And we all know power amplifiers (PAs) usually consume a major part of the energy in the system. For this reason if we can design a high efficiency PA, it will be of great help to improve the efficiency of the overall system.

Traditional linear power amplifier such as class-A or class-AB can achieve good linearity but their efficiencies are limited. To increase efficiency, class-F power amplifier is a good option. This kind of PA operates in saturation mode resulting in poor linearity. So it is not a good idea to use class-F PA directly in systems with varying envelop signals such as CDMA (code division multiple access) or WLAN. However, we can use these high efficiency power amplifiers in advanced transmitter architectures, for example, LINC (linear amplification using nonlinear components) or EER (envelop elimination and restoration) with digital predistortion [1].

Compared to traditional bulk CMOS technology, silicon-on-insulator (SOI) CMOS features higher speed and lower power consumption[2]. Moreover the high resistivity substrate beneath the buried oxide (BOX) layer brings high Q integrated inductor as well as excellent crosstalk isolation. Although it may have higher cost, SOI CMOS is a good choice for RF design[3].

This paper presents a high efficiency 1.9 GHz power amplifier designed using SOI CMOS technology. The power amplifier delivers 25 dBm output power with 20 dB power gain and 50 % PAE (power added efficiency) at 1.9 GHz.

II. POWER AMPLIFIER DESIGN

The proposed power amplifier is two-stage structure, which can achieve high gain and is not too complex. The two stages, drive stage and output stage, will be present separately.

A. Drive Stage

In power amplifier design, the drain voltage of the amplifier transistor can be as high as twice of the supply voltage, which may cause the serious breakdown problem. Cascode structure is a common method used to mitigate this problem. However, since the supply voltage of the thin oxide devices is as low as 1.5V, to further reduce the risk of breakdown, self-biased technique is adopted in this design.

As can be seen in Figure. 1, Transistor M2 is self-biased. In this case the drain voltage of M2 is fed back to M2's gate, so the voltage between drain and gate V_{dg} is reduced by 17 percent.

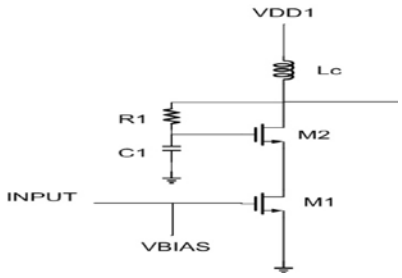

FIGURE I. .DRIVE STAGE.

B. Output Stage

For the output stage, thick oxide devices are used because they have higher breakdown voltage. And supply voltage is 2.5 V.

In most cases, the class-F power amplifiers are biased as class-AB or class-B state, and then we control the harmonics to shape the output voltage wave as square wave. Square voltage wave means the odd order harmonic impedances are infinite (besides the fundamental order) and the even order harmonic impedances are zero. At the output of the transistor, the second harmonic impedance should be zero and the third harmonic impedance should be infinite so as to obtain a proper ratio of voltage harmonics [4].

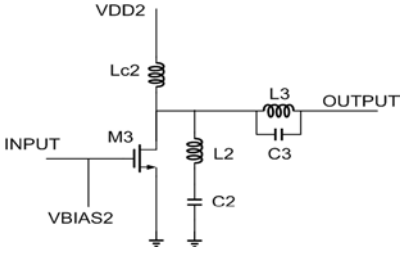

FIGURE II. OUTPUT STAGE.

To achieve this goal, a series resonate circuit and a parallel resonate circuit are implemented. In SOI CMOS technology, the inductors have higher Q factors than in normal bulk CMOS. For this reason, most of the capacitors and the inductors can be integrated on chip. But at the output of power amplifier, the inductors may cause a serious loss of output power and take large areas on chip. For this reason smaller inductors are preferred. To calculate the values of capacitors, we have following equations:

$$C_2 = \frac{1}{(2\times 2\pi f_0)^2 \times L_2} \tag{1}$$

$$C_3 = \frac{1}{(3\times 2\pi f_0)^2 \times L_3} \tag{2}$$

Where f_0 is the operating frequency (in this design f_0 is 1.9 GHz).

C_p is the parasitic capacitor of the transistor and L_{c2} is the RF choking inductor. To ensure the parallel of C_3 and L_3 being an open circuit, L_{c2} , C_p , C_2 and L_2 must form an infinite impedance by resonating at the third harmonic frequency.

$$Z_{Lc2} \square Z_{Cp} \square Z_2 = 0 \tag{3}$$

$$Z_{Lc2} = j3\times 2\pi f_0 L_{c2} \tag{4}$$

$$Z_{Cp} = \frac{1}{j3\times 2\pi f_0 C_p} \tag{5}$$

$$Z_2 = j(3\times 2\pi f_0 L_2 - \frac{1}{3\times 2\pi f_0 C_2}) \tag{6}$$

The C_2 and L_2 series is inductive at the third order harmonic frequency. Through some calculation we can get the equation below.

$$L_{c2} = \frac{L_2 - \frac{1}{(3\times 2\pi f_0)^2 C_2}}{(3\times 2\pi f_0)^2 (L_2 - \frac{1}{(3\times 2\pi f_0)^2 C_2}) C_p - 1} \tag{7}$$

By using this equation, the value of the RF choking inductor can be calculated and in this design it's 6.19 nH. Because this large inductor may cost too large chip area and bring power loss, it is off-chip.

With a matching network between the drive stage and the output stage, the overall power amplifier schematic is as shown below.

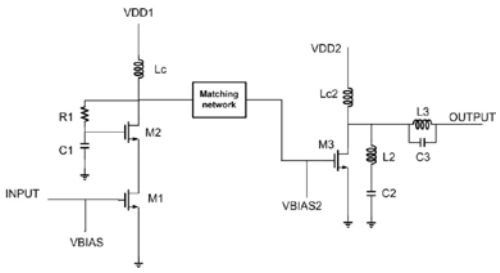

FIGURE III. THE OVERALL PA SCHEMATIC.

III. SIMULATION RESULTS

The present class-F power amplifier is designed and simulated by using Cadence. The working frequency is 1.9 GHz. Through load pull simulation, we conclude the optimized load impedance is around 10 Ω. Then a proper output matching network is needed as well.

The simulation results are as below. From Figure. 4, we can see the voltage and current waveforms at the drain of output stage transistor. The voltage waveform is almost square and the current waveform is half sinusoid.

Figure. 5 shows the output power of the PA and Figure. 6 shows the PAE curve. We can see that the output referred 1dB compression point is around 25 dBm and at this point the PA can achieve 50 % PAE.

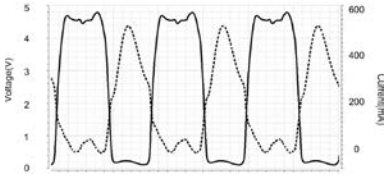

FIGURE IV. DRAIN VOLTAGE AND CURRENT WAVEFORMS (OUTPUT POWER IS 25DBM).

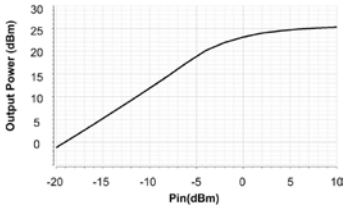

FIGURE V. OUTPUT POWER OF THE PA.

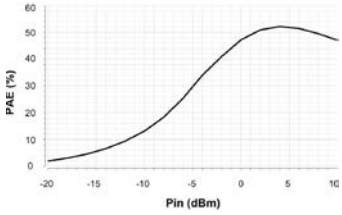

FIGURE VI. PAE OF THE PA.

IV. CONCLUSION

A 1.9 GHz class-F power amplifier in 0.18 μm SOI CMOS technology is present. By using cascode and self biased structure, we ensure the transistor not leaving breakdown region. By using series and parallel resonate circuits, a proper ratio of voltage harmonics is achieved, shaping the drain

voltage wave of the output transistor as square wave. The simulation results show that this PA can achieve 50 % PAE at the 1-db compression point of 25 dBm.

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REFERENCE

[1] A. Grebennikov. “High Efficiency Transmission Line GaN HEMT Inverse Class F Power Amplifier for Active Antenna Arrays,” Microwave Conference 2009, Singapore, Dec 7-10, 2009, pp. 317-320.

[2] F. Carrara, C. Presti, F. Pappalardo and G. Palmisano. “A 2.4-GHz 24-dBm SOI CMOS Power Amplifier With Fully Integrated Reconfigurable Output Matching Network,” IEEE Transaction on Microwave Theory and Techniques, vol. 57, pp. 2122-2130, 2009

[3] Y. Tan, M. Kumar, K. O. Sin, L. Shi and J. Lau. “A 900-MHz Fully Integrated SOI Power Amplifier for Single-Chip Wireless Transceiver Application,” IEEE Journal of Solid-State Circuits, vol. 35, pp. 1481-1486, 2000.

[4] D. Kang, D. Yu, K. Min, K. Han, J. Choi, D. Kim, B. Jin, M. Jun and B. Kim. “A Highly Efficient and Linear Class-AB/F Power Amplifier for Multimode Operation,” IEEE Transaction on Microwave Theory and Techniques, vol. 56, pp. 77-87, 2008.