Realization of FPGA-Based Video Image Fusion Technology

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***Abstract*—In order to achieve multiple video images fusion processing, domestic and foreign technology commonly used DSP to achieve image fusion algorithm, limited to serial instruction execution speed, it was difficult to meet the requirements of modern high-speed digital signal processing. An digital image fusion technology based on digital video decoder chip ADV7180 and FPGA hardware platform is presented, with high-speed analog input video signal is sampled by ADV7180, and the utilization of FPGA high-speed parallel signal processing capabilities, the image fusion technology can be implemented. The test results show that this method is simple and flexible, able to complete real-time image collection and image fusion.**

Keywords-video image fusion; ADV7180; image registration; pixel weighted average

I. INTRODUCTION

With the rapid development of digital image processing technology, image fusion technology has been widely used. The IKONOS from America implemented image fusion of high-resolution panchromatic images, multispectral images and SAR images, with the help of the image fusion technology, photographed objects were analyzed more accurate, national defense construction and economic development had a great raisement. We started later than foreign countries in terms of image fusion technology, a multi-ATC radar data fusion system was developed in Sichuan University, its performance had reached world advanced level, and was applied to domestic aviation management system successfully[1-3].

DSP was used typically as a traditional method to achieve image fusion, since the DSP processing speed was limited to its low sampling rate and its highest frequency the CPU could run. In this paper, ADV7180 video decoder chip completes high-speed sampling for input PAL signal, FPGA chip is used to complete image fusion processing. Due to abundant internal logic resources and strong high-speed parallel digital signal processing capabilities of FPGA, and FPGA chip can be configured flexibly and debugged online easily, FPGA chip has a smaller size, and is easily used to achieve a compact design, the cost for design and implementation can be reduced, the design efficiency can be improved[4-5].

II. PRINCIPLE OF IMAGE FUSION TECHNOLOGY

Image fusion technique utilizes the space-time correlation and the information complementarity of different detectors, processes and synthesizes the information from multiple sensors in multiple levels, completes more comprehensive and clearer description for the scene. Prior to image fusion, image collected by each sensors must be precisely registrated, and the registration accuracy would directly affect the image fusion effect.

A. Image Registration

Image registration refers to matching and superimposing two images or multiple images obtained from different sensors for the same scene. Existing image registration techniques at home and abroad mainly include fast image registration techniques, high-precision image registration techniques and automatic registration techniques.

By fast image registration techniques, real-time image registration can be completed quickly, but the techniques are generally limited by the hardware real-time processing speed. The error-precision for high-pricision image registration techniques is usually required to the sub-pixel level or deep sub-pixel level, but in practical applications, image acquisition is often disturbed by the noise impact, it is difficult to achieve high registration accuracy. Automatic registration techniques without human intervention, rely on computer to complete image registration automatically, but in many cases the registration process requires human intervention, automatic registration can not be completed [6-8].

In allusion to the shortcomings of traditional image registration techniques, and the characteristics of the image itself will not change due to the image translation, rotation and scaling, feature-based image registration method is used in this paper, and usually contains image feature extraction, image feature matching to complete image registration.

1) Image feature extraction. corner detection operator is used to complete the image feature extraction in this paper, by calculating the gray D-value squares in four different directions of the center pixel, a minimum gray D-value square can be obtained, the corresponding center pixel is the interest value, the corner is the maximal interest value compared with the pre-setting threshold.

Corner detection algorithm is more sensitive to the change of gray value, and has a high precision, simple algorithm and real-time performance.

2) The image feature matching and image registration. After the image feature point is extracted, image matching is completed with mutual relationship coefficient between two images, by selecting the appropriate translation, rotation and scaling transformation model, the image registration is completed with the nearest neighbor interpolation algorithm.

B. *Image Fusion*

After image registration is completed, the accuracy of the final image fusion can be ensured. According to different levels of which information is characterized, image fusion is usually divided into three treatment levels: pixel-level image fusion, feature-level image fusion and decision-level image fusion. Pixel-level image fusion is directed integrated in the original data layer, and the mothod is the lowest level image fusion, this method can retain as much as field data, and provide a richer, more accurate, more reliable information. Feature-level image fusion firstly extracts original information from various image sensors, then completes the feature information fusion. In the decision-level image fusion process, the preliminary ruling on the same target for each image sensors is established, and then the decision-level image fusion is made[9-10].

Considering the advantages and disadvantages of various image fusion algorithm, the pixel-level image fusion algorithm is used to complete image processing, this method acts directly on the image pixels, it is the most widely used image fusion technology in the field of image processing.

Pixel weighted average method, pseudo-color fusion and wavelet fusion algorithm are usually used in pixel-level image fusion, the fusion process technique based on pixel weighted average method is easily implemented in hardware. After comprehensive consideration, we use pixel weighted average method in this paper, and complete image fusion by the use of gray, pixel weighted average method is suitable for real-time image processing, and can effectively reduce the image noise.

Assumed that P1, P2 and P, respectively represent the two images to be fused and the fused image, according to the principle of image fusion, we can obtain the following expression:

$$P(i, j) = \omega_A P1(i, j) + \omega_B P2(i, j) \qquad (1)$$

ω_A and ω_B respectively represent the weight of two images to be fused, and met the equation $\omega_A + \omega_B = 1$. when two images have a high similarity, $\omega_A = \omega_B = \frac{1}{2}$, we can get pixel averaging method; when there is a big difference between two images, the image which has remarkable features should be assigned a greater weight, then we can get a better effect for noise suppression.

III. HARDWARE DESIGN OF IMAGE FUSION CIRCUIT

In this paper, EP4CE75 from ALTERA company is selected as the main processing chip for image fusion, ADV7180 video decoder chip from AD is used to complete the acquisition and conversion for PAL signal, IS61WV102416ALL SRAM memory chip from ISSI is utilized to implement the image data cache, the block diagram of image fusion circuit is expressed in Figure 1:

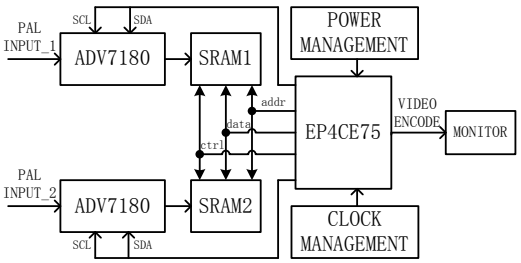

FIGURE I. BLOCK DIAGRAM OF IMAGE FUSION CIRCUIT.

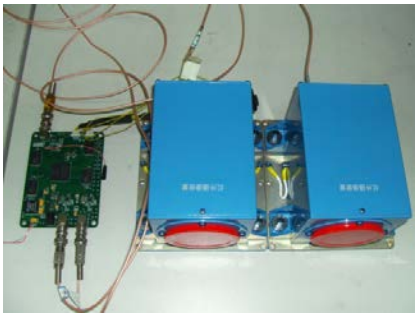

FIGURE II. IMAGE FUSION TEST EQUIPMENT.

In Figure 1, the two ADV7180 chips receive input analog PAL video signal to obtain output digital video signal by sampling-converting circuit and the video decoding circuit, the two SRAM chips are used to complete video data writing and reading, the data got out is utilized to implement image fusion with pixel weighted average method, then input the operation result to the video coding circuit, the final output PAL video signals can be observed on VGA monitor.

In order to verify the image fusion algorithm in this paper, we use the image fusion test apparatus in Figure 2, two horizontal infrared cameras are used to complete image acquisition for the same target, the image fusion board receives output PAL video image from the infrared cameras, the video decoding should be made firstly, then we implement image fusion.

IV. FPGA IMPLEMENTATION AND ON-LINE OBSERVATION

In this paper, Verilog HDL hardware description language is used for ADV7180 timing control and SRAM data reading and writing control with FPGA, after the functional simulation and verifying for FPGA program, the SignalTap logic analyzer integrated in Quartus II software is used to complete on-line observation for the input, output and internal signals. Then the system functionality is analyzed and verified with the data sampled and observed.

By the use of IIC protocol, FPGA chip can complete the registers configuration for ADV7180, the signal interactivity between ADV7180 and FPGA is shown in Figure 3:

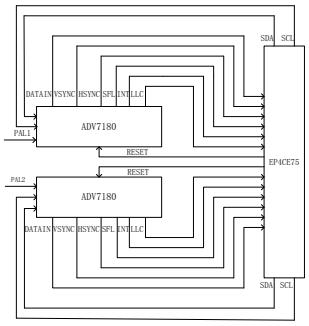

FIGURE III. SIGNAL INTERACTION DIAGRAM BETWEEN ADV7180 AND FPGA.

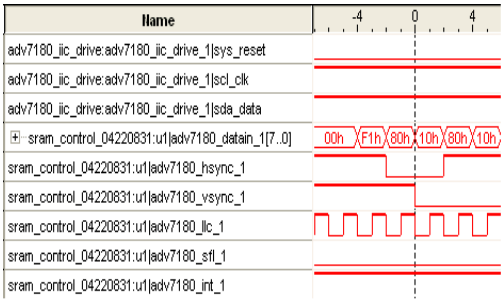

FIGURE IV. OUTPUT DIGITAL SIGNAL TIMING DIAGRAM FOR ADV7180.

In Figure 3, after the configuration for ADV7180 is completed, the input PAL signal is converted, then DATAIN, VSYNC, HSYNC, SFL, INT, LLC and other digital signals are outputted. the LLC signal is used as the sampling clock, and the 8-bit digital signal DATAIN is sampled, then the sampling data is utilized for subsequent image fusion. The on-line observation timing diagram for the output digital signals of ADV7180 is shown in Figure 4.

With the address signal and writing control signal sent by FPGA, the sampled data DATAIN is stored by address. When we read the data stored in the SRAM, the read address should be automatically adjusted according to the line offset and column offset required by image registration. In order to ensure the timing controllability for inter-clock domain operation, we use internal FIFO in FPGA to complete buffering operation, data read from the FIFO is used for pixel-level image fusion. Reading and writing control signal of SRAM, and the reading and writing control signals of FIFO are shown in Figure 5:

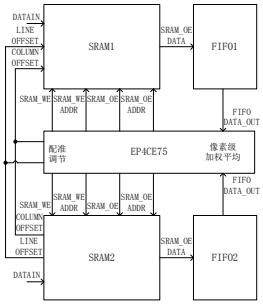

FIGURE V. READING AND WRITING SIGNALS INTERACTION OF SRAM AND FIFO.

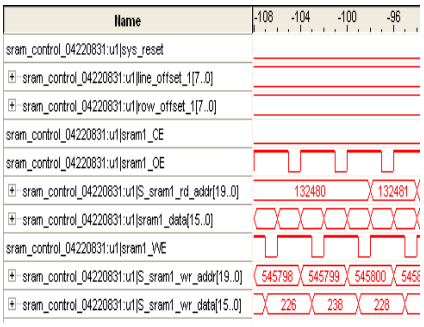

FIGURE VI. READING AND WRITING TIMING DIAGRAM FOR SRAM1.

Reading and writing signals of SRAM can be observed by SignalTap, reading and writing timing diagram of SRAM1 is shown in Figure 6, the row offset and column offset can be obtained according to the image registration adjustment, then we can calculate the corresponding address offset, data can be read from SRAM in linear address increment mode.

Data reading and writing of SRAM2 are executed in the same manner with SRAM1, data read from SRAM1 and SRAM2 is respectively sent to FIFO, data read from FIFO is used for pixel weighted average, and then the image fusion can be completed. After the key signal is analyzed and observed by SignalTap, we get the timing chart in Figure 7:

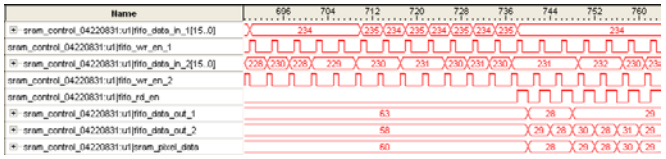

FIGURE VII. PIXEL WEIGHTED AVERAGE KEY SIGNAL TIMING DIAGRAM.

In Figure 7, fifo_data_in_1 and fifo_data_in_2 are input data of two FIFOs, fifo_data_out_1 and fifo_data_out_2 are output data for two FIFOs, the pixel weighted average of data read from two FIFOs is sram_pixel_data, the weight of data from two images is equal to 0.5.

V. RESULTS ANALYSIS AND VERIFICATION

Two-way output PAL video image data from infrared cameras is collected and stored in the computer, the collected data is lead to MATLAB simulation tools, then we get the simulation image as shown in Figure 8:

FIGURE VIII. SIMULATION GRAPHICS OF OUTPUT PAL VIDEO FROM INFRARED CAMERA.

FIGURE IX. SIMULATION GRAPHICS OF FUSED IMAGE.

Two-way PAL video data is used to implement image fusion in the FPGA chip, the processed image data is lead to MATLAB simulation tools, then we get the simulation image as shown in Figure 9.

Compare the image fused with the image to be fused, we can see that, through image fusion algorithm, the noise point of two-way test image data is effectively reduced, and the image information is more abundant and complete. After the quality of the fused image is evaluated in subjective evaluation method, we can see that the the fused image has a high quality.

VI. CONCLUSIONS

The principle of image registration and image fusion is introduced in this paper, image fusion hardware circuit is implemented in FPGA, after we complete image fusion for the two original PAL video signals sampled, experimental results show that the FPGA-based image fusion can complete the acquisition of PAL video images in real-time, and effectively eliminate noise point in the image, the image information is more abundant and accurate.

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