The Study of Real-Time Industrial Ethernet Power link Medium Redundancy

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Abstract--This paper analyses the medium redundancy technology in the Industrial Ethernet POWERLINK network. Ethernet data before heading to Media Access Controller, in order to achieve the medium redundancy, we design a Link Selector functional block, it can put three physical networks of the best quality network data to the Media Access Controller. This will ensure the robustness and stability of the physical network. The data delay is only a few microseconds time, does not affect the normal operation of network.

Keywords-link Selector; slot time; medium status; data jitter

I INTRODUCTION

Communication networks based on the IEEE 802.3 (Ethernet) protocol [1] are currently available for applications at all the levels of factory automation systems. In these industrial networks, particular attention has been dedicated to those capable of real-time performance, since they are suitable for employments at the "device" level of automation systems, where fast data exchange usually takes place between controllers and sensors or actuators. In such a context, they are commonly referred as Real-Time Ethernet (RTE) networks.

In this paper we focus on Industrial Ethernet POWERLINK (EPL), one of the most popular RTE networks. Industrial Ethernet POWERLINK is a communication profile for Real-Time Ethernet (RTE). It extends Ethernet according to the IEEE 802.3 standard with mechanisms to transfer data with predictable timing and precise synchronization. The communication profile meets timing demands typical for high-performance automation and motion applications [2].

With POWERLINK high availability, the availability of the system is ensured in the event of a component failure. Both the nodes and medium redundancy prevent having a single point of failure in the system. The use of several media carrying the same information at the same time ensures to be robust to any network component (cable, media convertor, hub...) failure.

The medium redundancy is achieved thanks to three different physical networks. Each node shall be linked to three physical networks via a Link Selector (this functional block is described in 2.2.1). All combinations of line and star (or tree) topology are allowed. The line topology will require external hubs or internal hubs with four ports.

II REDUNDANT NETWORK TOPOLOGY

As far as possible, the topology of both physical networks shall be identical (same number of hubs, same cable length). It

will ensure that a frame will reach a node on both links at the same time. Anyway, the difference of path delay between both links must not exceed $5.2\mu s$ (transmission time for the smallest Ethernet frame at 100 Mbit/s). The redundant medium network topology is shown in figure 1. Thus the first bits of a frame will be received on one link before the last bits of the frame will be transmitted on the second link. It will ensure that each node will be able to detect that a frame is present on both links or not.

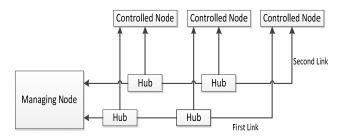


FIGURE I. REDUNDANT MEDIUM NETWORK TOPOLOGY.

Media Access Controller for each frame is a three port hub for the data forwarding. This means that a port into the data, and the other two ports for data forwarding (Forwarding a port data to Media Access Controller, another port data is forwarded to the next node). And right up to the Media Access Controller three-way data to choose the best data (Good quality data can be used to judge CRC) eventually given to the Media Access Controller.

IIILINK SELECTOR

In a redundant POWERLINK network, all nodes have to be connected to two different physical networks. Both physical networks shall convey the same redundant information. The Link Selector functional block is shown in figure 2. Each node has to transmit on both links and to select one link for reception. This function is done by the Link Selector functional block.

The Link Selector could be implemented within the POWERLINK node itself (Internal Link Selector), or within an external device connected to each POWERLINK node (External Link Selector). Each frame received from the controlled node (on the Protected Link), the Link Selector must simultaneously transmit this frame on the First and on the Second Link. Each frame received from the redundant network (on the First Link, or on the Second Link, or on both), the Link Selector must do a frame selection and transmit this

frame to the node on the Protected Link.

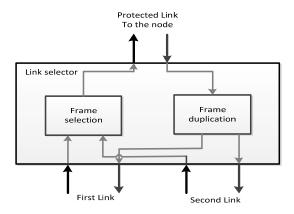


FIGURE II. LINK SELECTOR FUNCTIONAL BLOCK.

The selection mechanism could be as simple as selecting the first received frame. But more information could be taken into account for the selection (percentage of frames received with a bad CRC on each Link...). As the Link Selector shall be designed in the way to minimize the path delay and jitter increase, it should avoid having a store and forward mechanism. Note: When sending a frame in response to another one, special attention has to be paid to the maximum path delay (5.2µs). Otherwise collisions may occur.

IV NETWORK DATA FORMAT

POWERLINK manages the network traffic in a way that there are dedicated time-slots for isochronous and asynchronous data. Thus transmission of isochronous and asynchronous data will never interfere and precise communication timing is guaranteed. Data jitter is caused by the delay line, and the maximum jitter of less than 6 microseconds. In the three channels, the same slot in the frame is the same as. Two adjacent slot time data may be the same frame. The minimum value of slot time is stipulated as follows: slot time > Maximum frame long time + $2 \times data$ jitter.

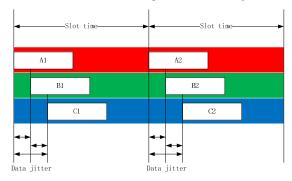


FIGURE III. REDUNDANT COMMUNICATION MEDIA DATA FLOW DIAGRAM.

The three networks redundant communication media data flow diagram is shown in figure 3. Each slot time, three way data select the highest quality to MAC. Data quality is indicated by the CRC check. Three way with a fixed priority, A road at the highest level, the C at the lowest level.

As can be seen from the figure 3, in the same slot time, the

data of three channels should be identical. If the CRC (Cyclic Redundancy Check) is correct, three channels should be the same value of the CRC. In same data channel, the data from two adjacent data frames are inconsistent, that result is inconsistent CRC. The judgment method: Set the value of slot time last CRC register previously-CRC selected data for the whole one. The slot time when judgment, if the CRC values consistent with previously-CRC register, this indicates that a data frame slot time within the same; if the CRC is inconsistent with previously-CRC register, it explained that it had to start the next slot time, and then need to refresh previously-CRC register. The receiving block diagram is shown in Figure 4.

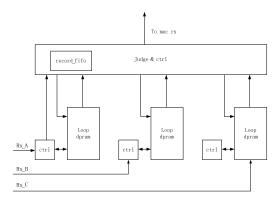


FIGURE IV. RECEIVING SCHEMATIC.

			1			1.1		
next state	Idle	Idle Preamable		D:	ata	Idle		
current state	Idle	Preamabl	е	Data		Idle	· ·	
wr_addr	XXX		load	load Load+1 ···.		Load+n		
rd_fist_addr	last					upda	updata	
Frame_length	XXX		0	0 +1		n		
Crc_OK								
RX_CRC	XXX		reset	Crc_		CRC		
Record_index	last					{frame_len	gth, last}	

FIGURE V. RECEIVING CRITICAL TIMING BLOCK DIAGRAM.

Receiving critical timing block diagram is shown in Figure 5. Reception scheme is described as follows: the signal Wr_addr is the address of this writing loop DPRAM(It's FPGA chip RAM). Storing this frame of the end of the address data, and then accumulate. Rd_first_addr: valid data on the end of a write address, update to the current wr_addr, when crc_ok is valid. Record_index: record the last write address: rd_first_addr and data length frame_length, while the choice of DPRAM number recorded together, stored records FIFO (First Input First Output), record_fifo when crc_ok signal is valid. Data recovery transmit state machine: In idle state as long as record_fif1 not empty it once a data recovery. First sends a preamble and SFD (Start Frame Delimiter), then read a record from record_fif0, in accordance with the recording {DPRAM number, read the data length, read the first address},

read from the corresponding loop DPRAM. Note: When crc_ok judgment, use has priority if else if the structure for fixed priority detected simultaneously on three networks crc effective when used. Crc compare crc register pre_crc on a slot time with, not equal, this indicates that the new data for the beginning of a new slot time, and for the first valid data frame; if they are equal, it expressed or this slot time for the data, and not the first valid data frame. If the new slot time data, then choose this path data, update pre_crc register, while generating entries record FIFO; if oriented sub- slot time data, discarding data.

V MEDIUM STATUS

The Link Selector shall provide information about medium status to the POWERLINK nodes, in order to inform the application of a medium failure. The medium status information will be introduced inside POWERLINK response frames (PollResponse, StatusResponse, IdentResponse) and request frame (PollRequest). In order to allow the detection of a cable issue in both directions (TX and RX) for each node, and to easily locate the medium failure, the Link Selector should set the medium status bits in the following way:

If the Link Selector is in front of (or inside) an AMN (SoC, SoA and PollRequest received from the protected port): For each response frame that is received from the redundant links, the medium status bits must be set according to the medium state at reception of this response frame.

If the Link Selector is in front of (or inside) a SMN or a CN (SoC, SoA and PollRequest received from the redundant For each response frame (PollResponse, StatusResponse, IdentResponse) that is received from the protected link (and so must be sent to both redundant links), the medium status bits must be set according to the medium state at reception of the request frame (PollRequest, StatusRequest, IdentRequest) on the redundant links. For each request frame (PollRequest) that is received from the redundant links, the medium status bits must be set according to the medium state at reception of this request frame. A Link Selector shall never reset a status bit which has been set by another Link Selector.

The bits 7 and 6 of byte 5 should be used in the following messages: PollRequest; PollResponse; StatusResponse (ASnd); IdentResponse (ASnd). A Link Selector must compulsorily include medium status information inside PollResponse. It may optionally include medium status information inside the PollRequest, StatusResponse and IdentResponse frames. Bit 7 = First Link Status (FLS) (0 = Link OK, 1 = Link not OK). Bit 6 = Second Link Status (SLS) (0 = Link OK, 1 = Link not OK). The byte 5 of these POWERLINK frame is the 19th byte in the Ethernet frame (not including 8 bytes of preamble).

In the following example, the Link Selector in CN2 has only received the request frame on the Second Link. The example of medium failure is shown in Figure 6. So the Link Selector inside the CN2 will indicate in the response messages (PollResponse, StatusResponse,) that First Link is in failure. The Link Selector inside the CN2 will also provide the medium failure information to CN2, setting the FLS bit of the PollRequest frame coming from the MN. The Link Selector

inside the MN will see both links ok, as a matter of fact it will receive the response of the CN1 and CN2 on both links. But as it will not reset the medium status bits, the application in the MN is able to detect that there is a medium issue between CN2 and MN.

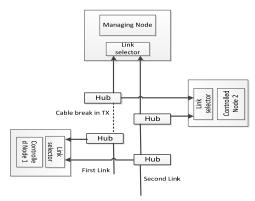


FIGURE VI. EXAMPLE OF MEDIUM FAILURE.

VI CONCLUSIONS

The medium redundant technology increases control system reliability and stability, which in the industrial control field has a wide range of applications. But since the data to the MAC before the judge on the first CRC, in a slot time to ensure that the MAC is a quality to the best data frame. This requires prior MAC data frame buffer. However, when playing a timestamp MAC PHY up data is not in a direct hit timestamp, but the data into the MAC timestamps. This introduces a small frame size has a relationship with each network latency, resulting in the delay do not be eliminated in the late synchronization. As a natural extension of this work, it is important to continue to study this how to solve the problems caused by delays.

ACKNOWLEDGEMENTS

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