Design and Implementation of the Fuze Circuit Board Tester

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***Abstract*-The system's objectives and tasks were clear by analyzing the system requirements. The front-end system was based on DSP (digital signal processor) and FPGA (field programmable gate array). It designed system communication protocolto control the testing process data switching. The PC software realized the whole test process. This test system mainly realized the followings: front-end power system design, signal waveform generation, measuring the echo signal from the circuit under test, automatically checking the measuring results and auto-generating the results reports. According to the test requires, it completed the schematic and PCB design of the front-end board. The signal generation algorithm and echo signal processing algorithm of DSP were wrotten through CCS, the test system timing, which FPGA controlled, used VHDL language to realize, and the whole test software was achieved by Lab windows/CVI. The software had friendly interface, elegant appearance, concise and was convenient and practical for users [1].**

Keywords- automatic test; DSP; FPGA; fuze

I. INTRODUCTION

Some devices are generally equipped with self-bombed device which could automatically explode under certain conditions. The automatic explosion is implemented under the control of the external command signal and this is the fuze. The role of fuze is to ensure the weapon systems which includes aerial bombs, atomic bombs, torpedoes, mines, grenades can detonate in the most favour able position. Correctness of electronic components determines the role of work in the war fuze played. Thus, the working condition for the fuze electronics components testing is necessary. The test of fuze circuit board and timely reparation of abnormal situation can guarantee the normal work of the fuze circuit board.

II. OVERALL PROGRAM DESIGN

A. Analysis of the System Test Requirements

The system is mainly to test echo signal and real-time working condition of the fuse board. The system is required toprovide the normal working voltage to the circuit under test, generate a dual channel of Doppler signal to drive the fuze board, test various logic signals automatically in the whole testing process or test each item independently, and produce a report of the testing result to be saved or printed.

B. Working Principle of the System

Working principle diagram of the system is shown in fig.1.After normal power supply of the testing system, the epigyn ous machine transmits the excitation wave signal to DSP through the serial port. According to the given algorithm, combined with the timing control of FPGA [2], DSP makes the processed data stored in RAM. Then the system restores analog waveform through the D/A conversion. After eased by signal conditioner and low-pass filter, the signal will be delivered to the fuze board which is being measured. When the fuze board is being driven, the system acquires output signal of the fuze board before a series of calculation and processing. At last, the testing results will be sent to epigynous machine through the serial port.

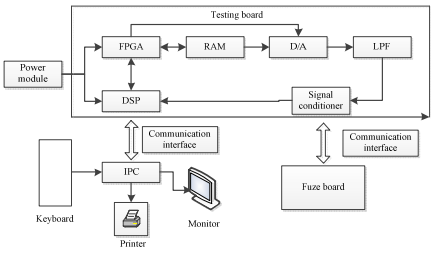

FIGURE I. WORKING PRINCIPLEDIAGRAM OF THE SYSTEM.

III. HARDWARE DESIGN

A. Power Module

The working voltage of various chip in the system have certainr equirements. The working voltages of DSP, FPGA, and RAM are 2.5V and 3.3V, at the same time, they are required to be 5V and 12V in the signal conditioner. In this satiation, the power supply system needs to go through two level conversions. The power management chip NCP117 made by ON Semiconductor Company is able to convert 220V into 12V, and then from 12V into 5V, 3.3V, and 2.5V. NCP117

NCP1117 is a1.0A low dropout fixed and adjustable voltage regulator. It can provide eight fixed output voltages which include 1.5V, 1.8V, 2.0V, 2.5V, 2.85V, 3.3V, 5.0V and 12V, while there are no minimum load requirements to maintain the normal operation of regulator. It also includes the version whose output voltages are programmable and adjustable from 1.25V to 18.8V by using two external resistors. The on-chip trimming can adjust basis or output voltage in the accuracy 1.0%. Internal voltage protection includes output current limiting safe operating area of compensation and thermal shutdown. In summary, Because of NCP117 series chips can meet the voltage requirements in this design and their low power consumption, it was selected as the system power supply converter. The power supply circuit was shown in fig. 2.

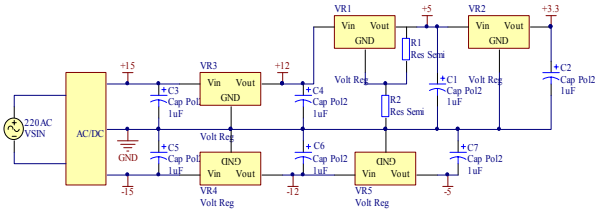

FIGURE II. THE POWER SUPPLY CIRCUIT.

B. Excitation Signal Generation Module

After the system provides enough working power for fuze board, an excitation signal wave needs to be generated to incentive the fuze board. Then if the fuze board works normally, it will feedback various signal information, which could be analyzed to estimate the working condition offuzeboard. The author has detailed the power module above, and now begins to introduce the principles and methods of generating the excitation signal waveform of the fuse board [3].

According to the requirements, system was asked to generate two channels of Doppler signal to drive the fuze board. Principle diagram of Implementation is shown in Figure 3.

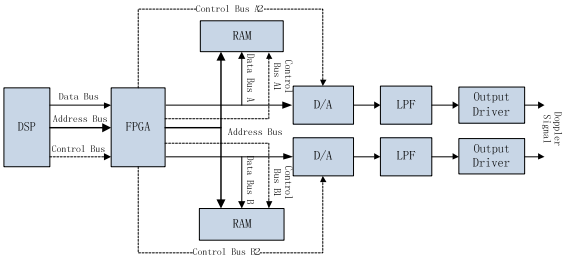

FIGURE III. TWOEXCITATIONWAVESIGNAL GENERATION PRINCIPLE DIAGRAM.

DSP is used to calculate the entireenvelope period, and the calculated value of each point is sent to RAM. Then system reads the value in RAM one by one according to a fixed frequency. Finally it completes the output of Doppler signal through D/A conversion.

On the basis of the system requirements, the carrier frequencies of Doppler signal are adjustable from 1.5 KHz to 120 KHz. In the condition of that it takes 2MHz clock as the output of RAM to D/A conversion by theoretical calculation, each period will have 16 outputs when the carrier is 120K.and at the same each period will have 1333 output when 1.5KHz. All of these can meet technical requirements in this system. In this way, a CMOS static RAM named IS61WV102416BLLwhose storage capacity is 1M×16 made by ISSI Company was selected as the storage device. Its working voltage is 3.3V and it has the advantages of high speed, high performance, low power consumption, speedup to 8ns, easily through the CE and OE memory expansion, and the expansion of development of memory can besubsequent applications.

Advantages of using this methodare more directto output Doppler signal, with acomplete outerenvelope for the output period. RAM with 1M×16storage space, outerenvelope with 500ms maximum time in a single period, system outputs continuous Doppler signal through the loop output. It is rather convenient that the definition of externalenvelopecan be arbitrarywave form. Compared with DDS method, the modulationprocess of this method has been done in the DSP, and all is converted into digital quantity. The calculation is more convenient and it only needs to output by D/A conversion. From this point of view, this method has more simple structure but most suitable for the design.

C. Signal Acquisition for Judging Module

Design of the measured circuit board's excitation signal has been successfully completed, and meets the system requirements. The fuze board has already gotten the excitation signal and it begins to run. On the one hand, the fuze board delivery its output signal to the signal interpretation and feedback circuit to be latched and analyzed for obtaining timing relationships and the measured value of multi-channel signal. On the other hand, testing system collects the output signals and sends them to the IPC for processing. As there is a large amount of workload in this test, here he author mainly studies and discusses the acquisition and judgment principle of several typical signal.

1) Power supply voltage and current measurement. Measurement circuit diagram of voltage and current is shown in Figure4.

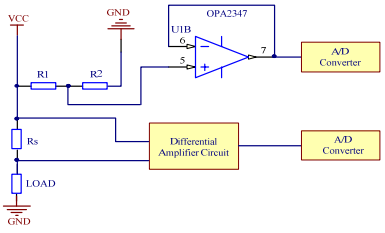

FIGURE IV. MEASUREMENT CIRCUIT DIAGRAM OF VOLTAGE AND CURRENT.

The measurement of the voltage is determined by both the size of the measured voltage and the measurement range of

A/D. The maximum voltage is 2.0V and measurement range is 2.5V in this circuit design. In this circuit, V_6 is equal to V_7, so V_5 and V_6 are equal. Thus R_1 and R_2 can be used to distribute the voltage of VCC which needs to be measured. Meanwhile, the current between point 6 and point 7 should be limited in the allowable range of operational amplifier OPA2347.When the VCC is -12V, it needs are verse amplification circuit by then accessing to a new level of operational amplifier.

Current range corresponding to 12V, 5.1V,-12V supply voltage are: 2~30mA,100~200mA,20~100,mA.They all need through the differentialamplifier circuit for amplifying. R_{LOAD} could share the voltage across R_S, and V_{Rs} can be controlled to be about 100mV. In the real circuit, the allowable maximum current is 150mA, so R_S can be configured as about 500mΩenough.

2) Super threshold signal NPLG, superthreshold signal detection NPLJ and nearexplosivefuzesignal UPF measurement.

Super threshold signal NPLG, superthreshold signal detection NPLJand nearexplosivefuzesignal UPF are all the typical signals in fuze board circuit measurement. Their amplitude and frequency need to be measured, and they must be in the prescribed value to illustrate the fuze board work normally. When measured through the front-end shaping circuit, the A/D converter and timer of DSP measure these signal's amplitude and frequency. Measurement circuit is shown in Figure 5.

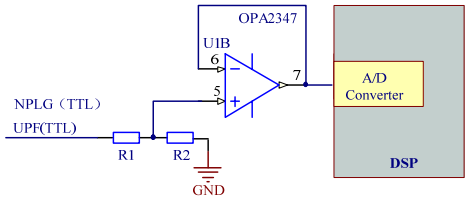

FIGURE V. MEASUREMENT CIRCUIT DIAGRAM OFNPLG AND UPF.

IV. SOFTWARE DESIGN

The software of the testing system can be divided into two layers, as shown in Figure 6.

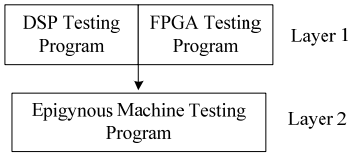

FIGURE VI. THE TESTING SYSTEM SOFTWARE HIERARCHY DIAGRAM.

In the first layer, DSP and FPGA use hardware structure of embedded system. So the DSP and FPGA testing procedure is the entrance of the whole testing system. They are responsible for the hardware initialization of the measured board and establish the necessary operating environment of the upper control program. DSP testing program is written by CCS software, and FPGA testing program with VHDL language, Development environment for ISE software. The program flow of the first layer is shown in Figure 7.

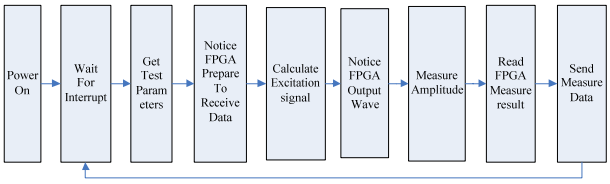

FIGURE VII. PROGRAM FLOW OF LAYER 1.

In the Second layer, the epigynous machine testing program is written by LabWindows/CVI [4] software.LabWindows/CVIis a typical VISA(Virtual Instrument Software Architecture). Its programming mode is simple and intuitive, and it can combine the flexible powerful C language platform with professional testing tools for dataac quisition, analysis and displayorganically. Integrated development platform, interactive programming method, and the rich library function, greatly enhances the C language function. It provides an ideal software development environment for the developers who is familiar with C language to establishdetection system, automatic measurement environment, data acquisition system, process monitoring system. The program flow of the second layer is shown in Figure 8.

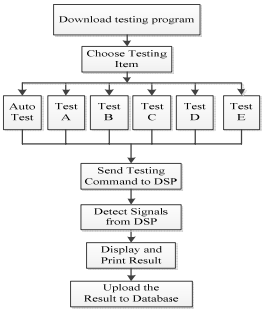

FIGURE VIII. PROGRAM FLOW OF LAYER 2.

V. SUMMARY

Fuze roles more and more significantly in the modern weapon system, and it has also developed rapidly in recent years. Therefore, to ensure the normal work of the fuze is particularly important. This papers pecifically aimed at the design of fuze measurement work to develop a set of testing system which is suitable for the measurement of fuze boardin weapon system. The development of the fuze circuit tester is starting from the whole, based on the current advanced embedded technology, in accordance with high reliability, high stability, simple operation principle, strictly following the requirements of the project, careful to design and optimize. Finally, through a large amount of testing and debugging work, the system is stable enough, and it meets the design requirements.

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