A track and hold circuit

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Abstract. A track and hold circuit is introduced, which includes a input buffer, a unit gain amplifier, a sampling switch, a current source, a driving NPN transistor and a over-driven protecting circuit. The over-driven protecting circuit is introduced to prevent the transistor of sampling switch from getting into linear working region. As a result, the sampling rate is improved dramatically. Meanwhile, two-stage insulation is adopted to prevent the incoming signal to disturb the holding signal on the sampling capacitor.

Introduction

Generally, track and hold circuits [1-4] are faster than the sample and hold circuits [5-9], because there is no settling time in the holding phase for track and hold circuits. A traditional track and hold circuit usually includes one or several input buffers, sampling switches, driving transistors and sampling capacitors. In the holding phase of the traditional track and hold circuit, the incoming signal is separated from the holding signal on the sampling capacitor only by one turn-off driving transistor which leads the strong coupling between the incoming signal and the holding signal. Furthermore, for traditional track and hold circuits, the transistor of the sampling switch gets into linear working region, which slows down the sampling rate dramatically.

In this paper, a new track and hold circuit is introduced, which includes a input buffer, a unit gain amplifier, a sampling switch, a current source, a driving NPN transistor and a over-driven protecting circuit. The track and hold circuit works periodically, driven by a clock signal. The working period is divided into two phases: tracking and holding phases. In the tracking phase, the sampling switch is connected to the emitter of the driving transistor. The incoming signal is first buffered by the input buffer, then, amplified by the unit gain amplifier, and through the driving transistor to charge the sampling capacitor. At the end of the tracking phase, the sampling switch is disconnected from the emitter of the driving transistor and connected to its base, which starts the holding phase. In the holding phase, the base of the driving transistor is pulled down to shut it off resulting the holding of the charges on the sampling capacitor. Because of the adoption of the over-driven protecting circuit to prevent the transistor of sampling switch from getting into linear working region, the sampling rate is improved dramatically. Meanwhile, two-stage insulation is adopted to prevent the incoming signal to disturb the holding signal on the sampling capacitor.

Circuit

As shown in figure 1, the proposed track and hold circuit consists of a input buffer B1, a unit gain amplifier, a sampling switch S1, a current source U3, a driving NPN transistor N4, a sampling capacitor C1 and a over-driven protecting circuit.

Furthermore, the unit gain amplifier consists of two NPN transistors N1 and N2 and two current sources U1 and U2. The two NPN transistors N1 and N2 form a differential pair with U2 as its tail current source and U1 as its sourcing load. The output of the unit gain amplifier is feedback to one of input of the differential pair and the other input is connected to the output of the input buffer B1. In order to set the unit gain amplifier in the best working condition, the magnitude of the current of U2 is designed to be two times that of the current of U1.

Furthermore, the over-driven protecting circuit consists of a PMOS transistor P1, a current source U4, a NPN transistor N3. A source follower is formed by PMOS transistor P1 and current source U4. The input end of the source follower is connected to the top plate of the sampling capacitor C1 while its output end is connected to the base of NPN transistor N3.

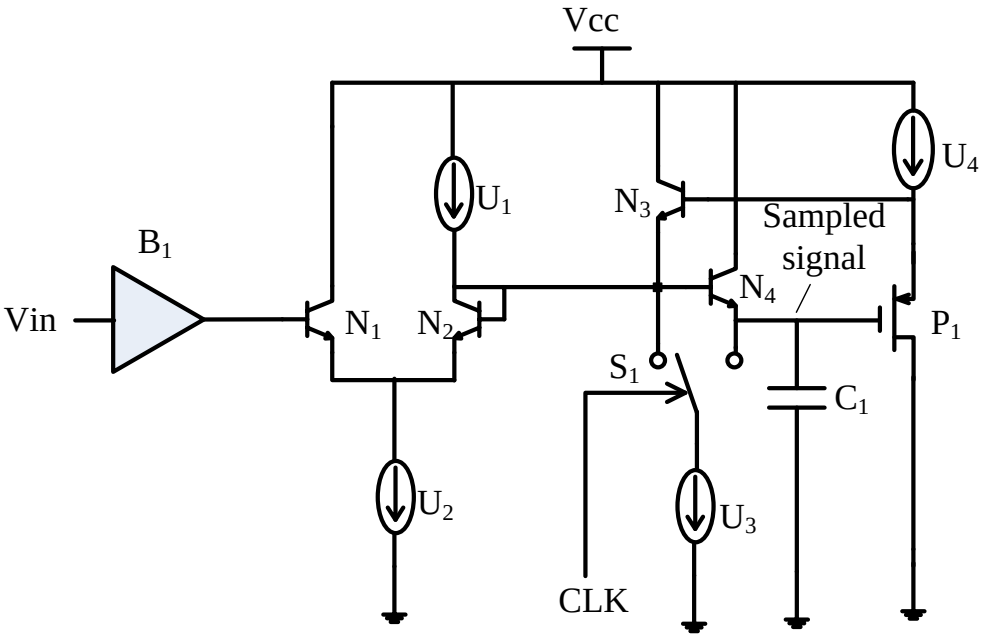

Figure 1. Proposed track and hold circuit.

Working principle

Driven by a clock signal CLK, the proposed track and hold circuit works periodically. The working period can be divided into two phases: tracking and holding phase. In the tracking phase, the switch S1 is driven to the emitter of the driving NPN transistor N4. As a result, an emitter-follower is formed, which consists of driving NPN transistor N4 and current source U3. The incoming signal Vin is first buffered by B1, then amplified by the unit gain amplifier, and through the emitter-follower charges the sampling capacitors C1. The base-emitter voltage of NPN transistor N3 is

$$V_{be3} = |V_{GS}| - V_{be4} \tag{8}$$

where V_{be4} is the base-emitter voltage of the driving NPN transistor N4 and V_{GS1} is the gate-source voltage of the PMOS transistor P1. The magnitudes of the first and second terms on the right side of equation (1) are almost equal, so V_{be3} is samll, which means at tracking phase the NPN transistor N3 is turned off, which won't influence the normal working of track and hold circuit.

At the end of the tracking phase, a change of CLK signal happens which disconnects the sampling switch from the base of driving NPN transistor N4 and connects it to the output of the unit gain amplifier, which pushes the track and hold circuit into holding phase. The current of U3 is designed to be far bigger than that of U1, so the potential level of the base of N4 is pulled down until N3 is turned on and supply as much current as

$$Ie3 = I3 - I2 \tag{8}$$

where I3 and I2 are the currents provided by U3 and U2, respectively. As its base is pulled down, N4 is turned off and the charges on capacitor C1 is held, since there is no path for the charges to leak away. The output of the unit gain amplifier is pulled down too, so N2 is turned off too, which further separates the incoming signal Vin from the holding charges on C1. The appearance of N3 prevents the NPN transistor in S1——which is always a differential pair of two NPN transistors as shown in figure 2——from getting into linear working region, which will slow down the switching speed dramatically.

Measurement

The proposed track and hold circuit is made in a BiCMOS process. The measurement shows that the proposed track and hold circuit has performances of 2.5GSPS sampling rate, 68dB SNR, 10 bits ENOB, and 77 SFDR, which can meet the requirement of 14-bit ADC, as shown in figure 3.

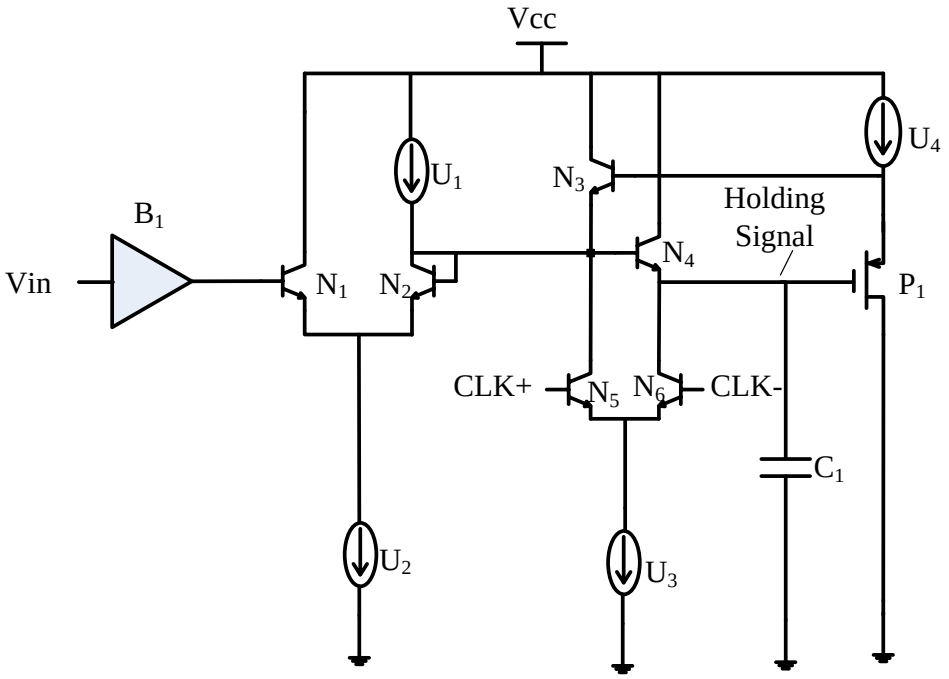

Figure 2. A NPN differential pair works as sampling switch.

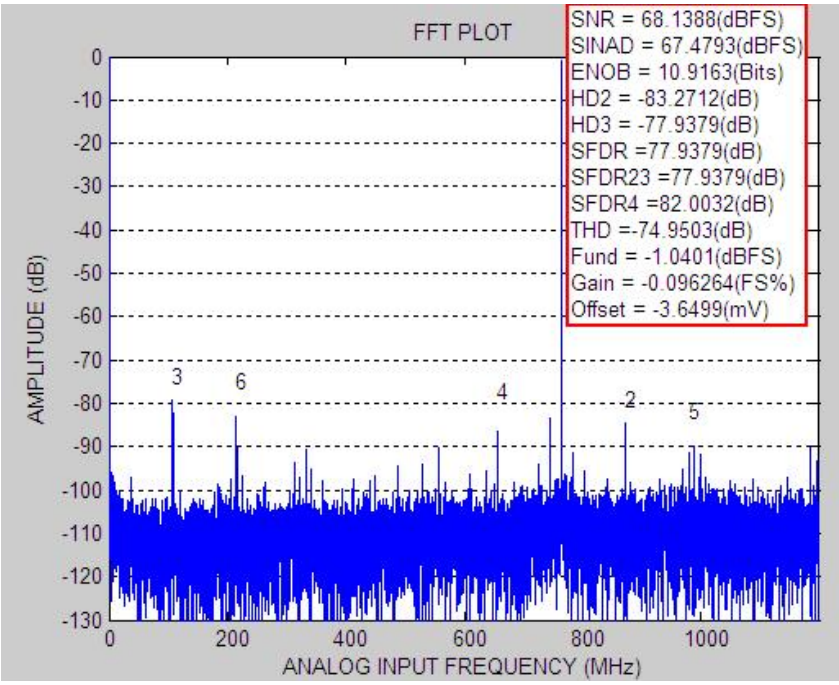

Figure 3. Measured performances.

Conclusion

The proposed track and hold circuit includes an input buffer, a unit gain amplifier, a sampling switch, a current source, a driving NPN transistor and a over-driven protecting circuit. The over-driven protecting circuit is introduced to prevent the transistor of sampling switch from getting into linear working region. Meanwhile, two-stage insulation is adopted to prevent the incoming

signal to disturb the holding signal on the sampling capacitor. The measured performances show that the proposed track and hold circuit can achieve a sampling rate of 2.5GSPS, which is almost two times that of traditional track and hold circuit. Beside, other specifications are also better than that of traditional one.

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