The Application of Clock Synchronization in the TDOA Location System

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Abstract. In order to solve the problem about the clock synchronization and high precision in the TDOA location system, a clock synchronization scheme was designed. In the article, the GPS+TCXO clock module was used as the front end of the reference clock source, and the PLL + clock buffer solution was used in the back end. The effect of the clock and ADC was analyzed on the TDOA location system; the system hardware designs were analyzed, such as the selection principle of the reference clock source and the PLL clock hardware circuit design and the parameter selection basis; the synchronous sampling method of the system clock and the register allocation process through the FPGA logic were introduced. The experimental result showed that the proposed scheme can reduce the clock jitter and improve the accuracy and stability of the input clock.

1 Introduction

The most important content in radio management is the monitoring of the radio emission source, and the accurate positioning of the unidentified transmitting source. The main positioning methods are two major categories: one is the composite angle positioning method, and the other is the time difference method. Based on the radio direction finding, the composite angle positioning method can be carried on the direction findings by using the multi-radio monitoring stations. The correlation interferometer and the Watson-Watt direction finding system are often used in the current direction finding systems; for the antenna device, their consistency requirements are needed relatively high; for the same frequency and multipath signal ,their distinguish ability are poor. the traditional monitoring methods can not meet the high miniaturization, convenience ,flexibility and precision positioning demands in current.

Time Difference of Arrival (TDOA), which is based on the signal arrival time to the monitoring station, locates signals through the conversion between time and distance; and it is a multi-sites positioning system, the signal location system must be more than three monitoring stations . The composition of each monitoring station is relatively simple, including the receiver, antenna and time synchronization module. In theory, the existing monitoring station only has the time synchronization module upgraded to become a TDOA monitoring station, without the need of complex technical transformation [1].

The TDOA location method has two major problems, the first is the multi-station time synchronization problem, namely the problem is the synchronous sampling of signal; the second is the time difference estimation between different stations; by the development of digital signal processing algorithm, the precise TDOA estimation becomes possible [2]. In fact, the essence of the two problems is the accuracy of clock synchronization. At the same time, the accuracy of the clock also affects the dynamic range of the receiver's ADC.

In order to meet the TDOA location system's high precision and clock synchronization demand characteristics, a global positioning system (GPS) is proposed to provide a reference clock by combining with the characteristics of the existing clock technology, the LMK04031 and the LMK01000 clock chips are used to provide the low-noise jitter clock without the need for high-performance voltage controlled crystal oscillators (VCXO) module.

2 The Analysis and Design of the Clock Synchronization Scheme

2.1 The Clock Index and the Dynamic Range of the ADC

The jitter of the clock is the corresponding edge shift by the time length of the actual output clock signal relative to the ideal signal. The percentage of frequency or the absolute time values can be used as a measure of jitter. The clock jitter is the time domain representation of the phase noise. The phase noise is a description of the phase jitter and the phase modulation of the signal in the frequency domain; accurately speaking, it's the change quantity of the clock relative to its carrier frequency ,and also is the function of the carrier frequency offset. In fact, the time jitter and phase noise are the same description of the clock's characteristics from time domain and frequency domain respectively[3].

The clock signal is very important in the ADC sampling system, because the distortion of the clock signal can cause the error of the sampling results. The main factor of the performance in the test system is the clock jitter. The clock jitter is refered to the difference between the two clock cycles[4]. The principles about the Clock jitter effecting the performance of ADC can be roughly interpreted as the clock source jitter will enable the internal ADC circuit trigger error sampling time. As a result, the analog input signal is sampled in the error amplitude, thereby reducing the ADC SNR. ADC is driven by a certain clock signal, and its signal-to-noise ratio (SNR) is related to the jitter of the clock:

$$SNR = 20\log10\ (1/\ (2 - f*Tj)) \quad (1)$$

In the type, the f is the frequency of the input signal for the ADC, Tj for the clock jitter. From this formula, the quality of the clock signal can directly affect the test results of the ADC performance parameters. SNR is one of the important factors that affect the accuracy of time difference estimation.

Because the design clock is used in the TDOA location system, so the time domain characteristic of the clock output is measured by the clock jitter. The focus of the synchronization clock in this system is to design a circuit that can generate the low jitter and synchronous clock.

2.2 Synchronous Clock Analysis in TDOA Location System

The basic principle of the TDOA algorithm is to calculate correlation, and then gets the time difference. There are strict requirements for synchronization, and the synchronization includes the sampling start time, the sampling interval and the receiving frequency of the two receivers. Therefore, the sampling sequence of the two received signals is strictly aligned after A/D conversion. Here the sampling sequence alignment has two meanings. First, the sampling time interval is the same as the sampling frequency. Secondly, the sampling start time of the two wave signals are synchronized [5].

In view of the fact that the space positions of the receivers are different, the synchronization of the sampling clock becomes a very important problem. The deviation of the external clock will have a great impact on the following processing. The electromagnetic propagation time of the tens of kilometers corresponds to the μs level, so the corresponding TDOA's time difference accuracy should be reached to the ns level, and that the corresponding synchronization time or the frequency deviation can be needed to reach the order of 10^{-9}.

In view of the above analysis, the start time synchronization of the sampling signal was completed through the global positioning system (GPS), the receiver was added the GPS to get a high precision time standards, the time accuracy can reach to 15ns, and the impact on the time delay estimation can be ignored in this situation. This TDOA location system used a reference clock provided by GPS, the ADC sampling clock and other system clock was synchronized with the GPS clock, to ensure the whole system clock synchronization, and thereby reduce the effect of clock jitter and drift.

2.3 Clock Synchronization Scheme Design

Since the GPS can provide accurate time information, the short-term stability of the reference source is poor, and the impact of the external interference will cause the reference second pulse to

generate a large jitter. The clock provided by TCXO has good short-term stability, but the long-term stability is poor. Thus through the GPS provides a 1PPS reference to correct the frequency of TCXO, which forms a stable 1PPS and 10MHz reference source; then the required clocks are produced through the corresponding PLL clock and clock buffer. The clock synchronization scheme is shown in Figure 1.

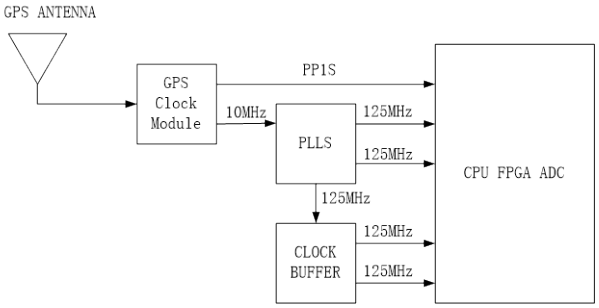

Fig.1. Clock synchronization scheme

3 Hardware and Software Design of the Clock System

3.1 Reference Frequency Selection for Synchronous Clock

The reference frequency source can provide a standard for the PLL, so it has a direct effect on the accuracy and stability of the output frequency. Crystal oscillator is often used as a reference source. The PLL frequency synthesis is essentially a frequency doubling of the reference frequency, and the frequency multiplication has an effect on the phase noise. Therefore, the selection of reference source with high stability and low phase noise can improve the output phase noise of the system. The design used the GPS module of the Thunder BoltE, this module got a time through the GPS and tamed the OCXO by the 1PPS, then provided the 1PPS and 10MHz clock reference, and the time accuracy can reach 15ns.

3.2 Hardware Circuit Design of the Synchronous Clock

PLL used the two-stage phase locked loop in LMK04031, and multiplied the corresponding 10MHz reference clock; In order to provide a clean and stable clock, the LMK04031's first order PLL was used to remove the near end interference and the second order PLL is for the distal filtering, and was distributed by LMK01000 clock buffer, which provided CPU and Serdes for FPGA, as well as ADC as the working clock.The schematic diagram of the clock PLL is shows in Fig.2.

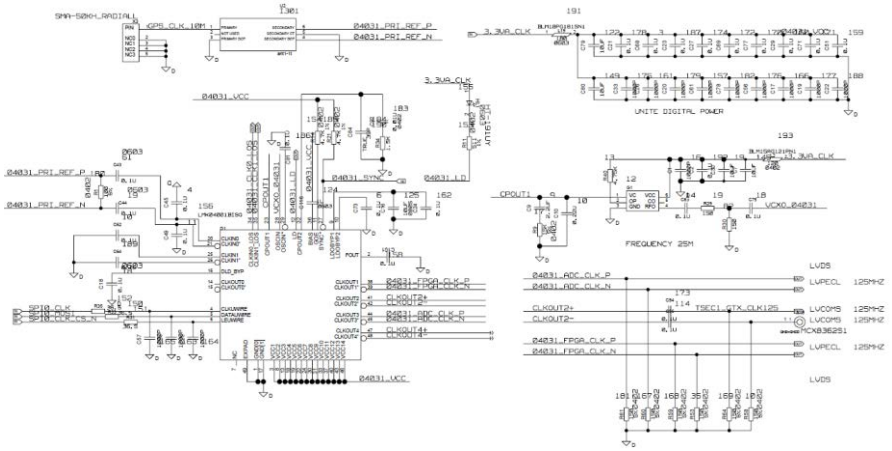

Fig.2. Schematic diagram of the clock PLL

The LMK04031 chip consists of two high performance synthesizer blocks (Phase Locked Loop, internal VCO/VCO Divider, and loop filter), source selection, distribution system, and independent clock output channels. The Phase Frequency Detector in PLL1 compares the divided (R Divider 1) system clock signal from the selected CLKinX and CLKinX* input with the divided (N Divider 1)

output of the external VCXO attached to the PLL2 OSCin port. The external loop filter for PLL1 should be narrow to provide an ultra clean reference clock from the external VCXO to the OSCin/OSCin* pins for PLL2. The Phase Frequency Detector in PLL2 then compares the divided (R Divider 2) reference signal from the PLL2 OSCin port with the divided (N Divider 2 and VCO Divider) output of the internal VCO. The bandwidth of the external loop filter for PLL2 should be designed to be wide enough to take advantage of the low in-band phase noise of PLL2 and the low high offset phase noise of the internal VCO. The VCO output is passed through a common VCO divider block and placed on a distribution path for the clock distribution section. It is also routed to the PLL2_N counter. Each clock output channel allows the user to select a path with a programmable divider block, a phase synchronization circuit, a programmable delay, and LVDS/LVPECL/2VPECL/LVCMOS compatible output buffers.

ADI PLL design software ADISIMPLL was used to design the loop, and can determine the loop filter based on the loop bandwidth, phase discriminator frequency, phase margin. Loop 1, used a 10MHz OCXO as reference frequency, selected a 25MHz VCXO,R1 and N1 frequency divider respectively were 20 and 50, the phase discriminator frequency were 500KHz, loop bandwidth were selected about 1/10 of the phase discriminator frequency, so the loop bandwidth of the filter were selected to 50KHz.The LMK04031's internal VCO frequency is 1430 to 1570 MHz, the output is set to 1500MHz, after 3 frequency divider by DIVIDER VCO and 4 frequency divider by the multiplied channels ,a 125MHz clock can be output. The reference input of Loop2 was the output of the loop1's VCXO output which was 25MHz, the VCO output 1500MHz. the frequency divider R2 and N2 values were 200 and 400, the phase discriminator frequency were 125kHz, the bandwidth of the loop filter2 were 12.5kHz.

3.4 System Synchronization Clock Software Design and Configuration

3.4.1 1PPS Synchronization Scheme

The GPS second pulse front and the standard UTC moment are aligned. So in second pulse production, the time of the system is the most accurate. The GPS data were transmitted from the serial interface to the TDOA location system, and the time delay can be changed and become long [6]. So the current time can be got by adding a second to the last time. At the same time, the TDOA location system time can be update, which can improve the time transfer accuracy.

3.4.2 Logic Configuration of Clock Chip

The value of the register can be determined by the TI software CODELOADER. This design used the FPGA to configure the registers.

After the system normal powered up, the state machine was in the idle state of the C_IDLE; when the system received a initialization signals, the state machine jumped to the C_START state; and then the system jumped to the C_INTERFACE state, if the two clock interface configuration was complete, the state machine jumped to C_IDLE, or jumped off the state machine of the C_REG for register configuration; in the C_REG state, by determining whether the register configuration was complete, it returned to the status of the C_INTERFACE, or jumped to the next state of C_BITSTART; then the configuration byte jumped to the C_BIT_DATA state of a single register configuration if the 32 bit configuration was complete , the state machine jumped to the C_BIT_LATCH state; in the C_BIT_LATCH state, the clock chip latched the writing data, then the state machine came into the C_BIT_OVER state; in the C_BIT_OVER state, a register allocation process was over, then jumped to the C_REG state for the next register configuration. The state machine of the clock chip was converted as shown in Fig.3.

The time sequence simulation waveforms about the corresponding register configuration are shown in Fig.4. As can be seen, the S_state_next and S_state_current variables were assigned different values according to the external trigger signal S_spi_config_start, which made the state machine of the system jump; S_interface_cnt interface counter, S_reg_cnt register counter, S_bit_counter bit counter were as a trigger condition of the state machine to jump; thus the outputs signals of O_spi0_clk_cs_n, O_spi0_clkbuf_cs_n, O_spi0_clk, O_spi0_mosi were as the clock's configuration SPI interface .

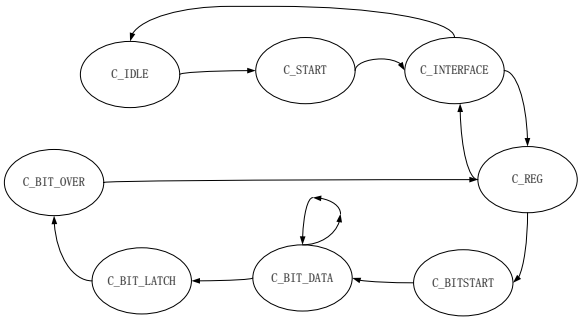

Fig.3. State machine conversion of the clock chip

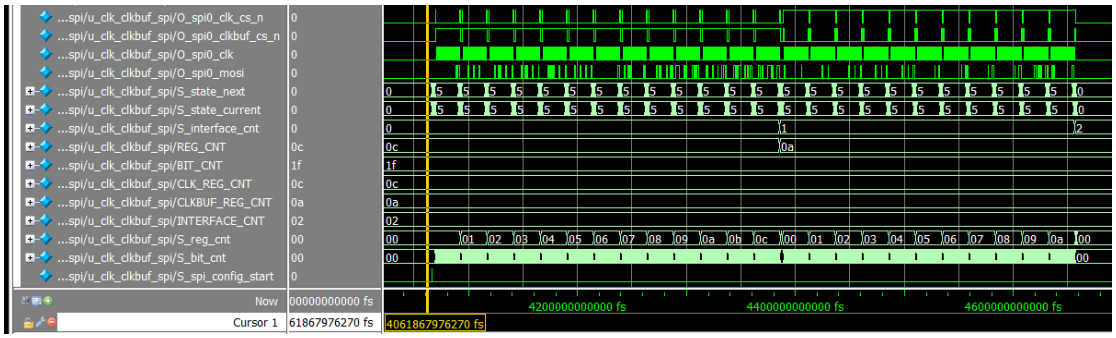

Fig.4.The simulation waveforms of register configuration

4 Synchronous Clock Test

By using the aforementioned method to design the corresponding clock synchronization system, and testing the front end reference clock 10MHz and the PLL 125MHz by high speed oscilloscope, the results were shown in Fig.5 and Fig.6.

By comparing the two pictures, it can be seen that the clock jitter and the harmonic components of the clock jitter were obviously decreased by the clock PLL. And according to the oscilloscope's test report ,it showed that the clock jitter had been reduced from 1.4547ns to 49.132ps. It showed that the clock synchronization system was effectively filtered out of the near and remote phase noise of the clock, which reduced the clock jitter and met the requirements of the system clock.

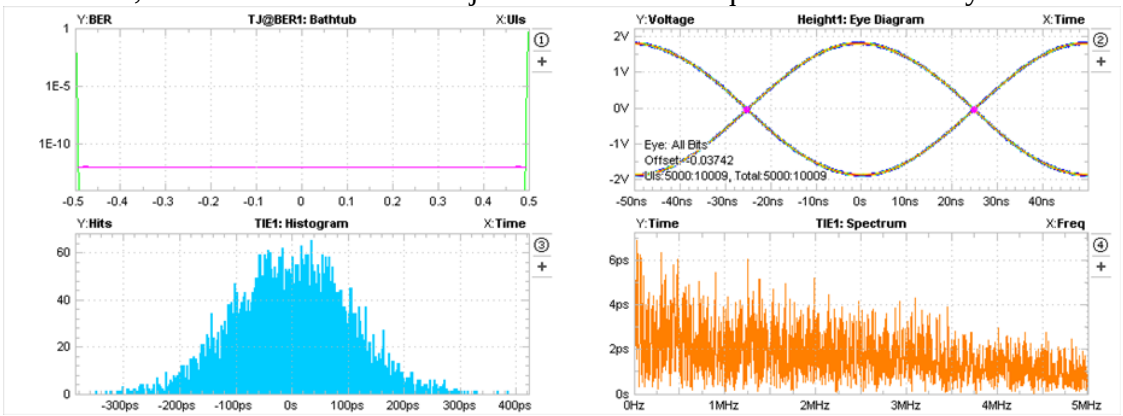

Figure .5 .10MHz clock's bathtub, eye diagram, histogram and spectrum

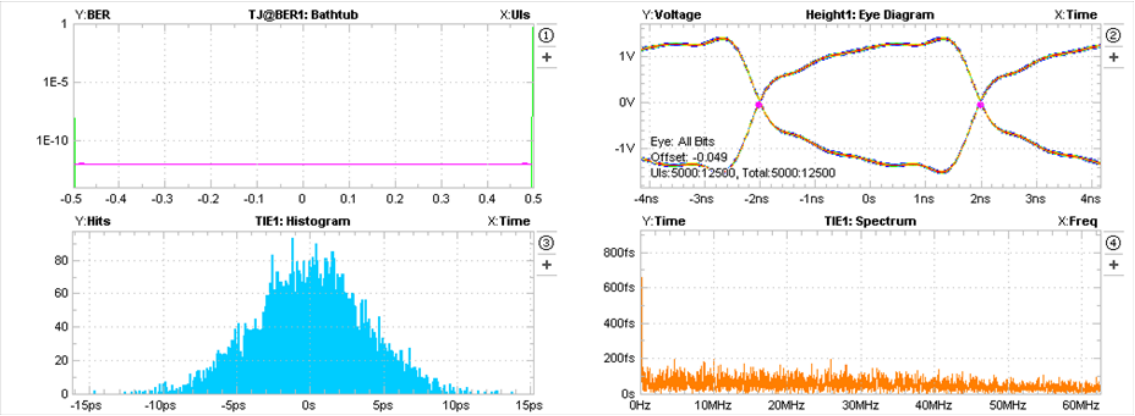

Figure .6 . 125MHz clock's bathtub, eye diagram, histogram and spectrum

5 Conclusions

In this TDOA location system, it used the GPS module to offer the 1PPS and 10MHz clock; the 1PPS clock was used as the start time of the synchronous sampling, the 10 MHz clock was used to provide a reference for the PLL clock chip LMK04031, and through the clock buffer chip LMK01000 was for clock distribution. The problems of clock synchronization in TDOA location system were solved. By testing the corresponding clock index, the system can meet the requirements of the clock quality and synchronization accuracy. At the same time, the clock synchronization design scheme has an important engineering guidance and reference value for the other high precision clock design.

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