A General Analytical Calculation of DC-Link Current and Voltage Ripple for 3L-NPC-Voltage Source Inverter

Xuebing Pei[1, a]

[1]China Ship Development and Design Center, Wuhan, 430064, China

[a]email: peixbhust@163.com

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Abstract. In this paper, a general analytical calculation of dc-link current and voltage ripple is presented for three-level three-phase neutral-point-clamped voltage source inverter (3L-NPC-VSI). Based on the analysis of average dc-link current of the upper and lower switches, the low-frequency oscillation of the neutral point (NP) voltage can be eliminated by injecting a zero sequence component. Moreover, the general expression of the root-mean-square (RMS) dc-link current is derived. In addition, the dc-link average current, rms current, and voltage ripple of the 3L-NPC-VSI are compared with those of the 2L-VSI, and it shows similar dc-link characteristics. Simulation results are shown to verify the theoretical analysis. The results can be extended to any PDPWM with NP voltage control strategy.

Introduction

Multilevel converters have drawn tremendous interest in the power industry, transportation, and renewable energy [1]. Among these topologies, the three-level three-phase neutral-point-clamped voltage source inverter (3L-NPC-VSI) shown in Fig. 1 is the most popular one [2]. For proper operation of this topology, the modulation strategy must be designed to achieve voltage balancing between upper and lower capacitors [3]-[6]. Although the neutral-point (NP) voltage balancing can be achieved, the derivation of the algorithm is difficult to understand, due to the complex calculation of the NP current. Moreover, the general expressions of average and root-mean-square (rms) dc-link current and voltage have not been derived for 3L-NPC-VSI, although the dc-link current ripple analysis has been investigated for PWM-VSI [7]-[8].

In this paper, a general analytical calculation of dc-link current and voltage ripple is presented for 3L-NPC-VSI. It is found that the low-frequency NP voltage oscillation can be eliminated on the basis of the analysis of the average dc-link current. Moreover, both 2L-VSI and 3L-NPC-VSI show similar dc-link characteristics, in terms of the average current, rms current, and voltage ripple. Simulation results are shown to verify the theoretical analysis.

Circuit Analysis of 3L-NPC-VSI

Fig. 1 shows the topology of a traditional 3L-NPC voltage inverter. The inverter bridge and load can be simplified as a current source i_{dc} in the equivalent circuit as shown in Fig. 2. The constant dc current comes from the DC source due to the infinite impedance of the capacitor for dc frequency. The capacitor C_{dc} (total dc-link capacitance) and inductance L_{dc} constitute the LC filter to attenuate the harmonic current through the DC source.

From Fig. 1, the dc-link current $i_{dc,up}$ and $i_{dc,down}$ of 3L-NPC-VSI are determined by

$$i_{dc,up} = S_{Qa1}i_a + S_{Qb1}i_b + S_{Qc1}i_c \tag{1}$$

$$i_{dc,down} = S_{Qa4}i_a + S_{Qb4}i_b + S_{Qc4}i_c \tag{2}$$

where i_a, i_b, and i_c are the output currents of the inverter bridge, and S_x (x represents the switches Q_{a1}, Q_{a2}, etc.) are the switch functions, respectively.

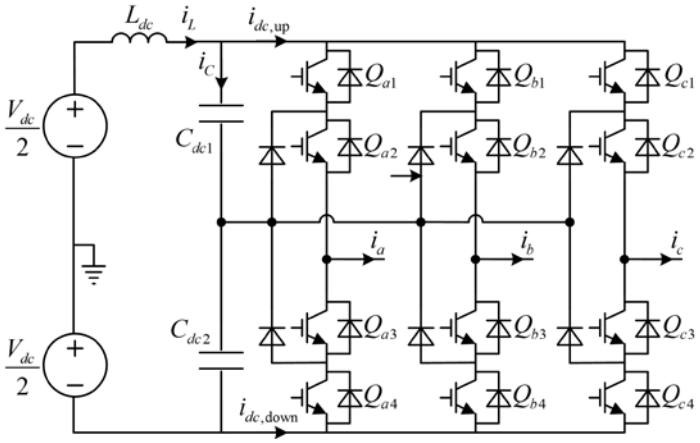

Fig. 1: 3L-NPC-VSI topology.

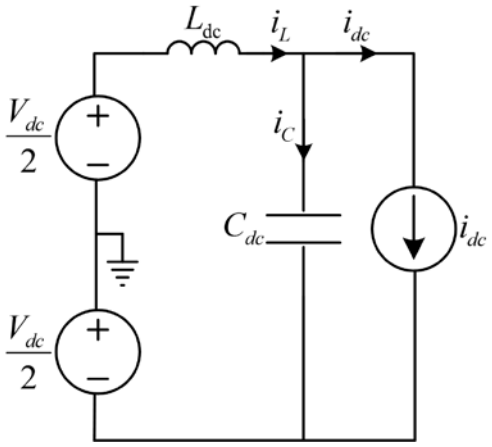

Fig. 2: Equivalent circuit for dc-link.

Average and RMS Values of DC-Link Current

A. Average Value of DC-Link Current

The traditional SPWM three-phase reference voltages $v_{x,ref}$ (normalized w.r.t $V_{dc}/2$) and the corresponding duty cycles δ_{x1} and δ_{x4} for 3L-VSI are given by (3) and (4) below respectively

$$v_{x,ref} = m\cos(\theta + \theta_x) \tag{3}$$

$$\delta_{x1} = \begin{cases} v_{x,ref}, & if\ v_{x,ref} \geq 0 \\ 0, & if\ v_{x,ref} < 0 \end{cases} \qquad \delta_{x4} = \begin{cases} 0, & if\ v_{x,ref} \geq 0 \\ -v_{x,ref}, & if\ v_{x,ref} < 0 \end{cases} \tag{4}$$

Where m is the inverter modulation index, and x for phases a, b and c. Especially θ_x is equal to $\theta_a = 0$, $\theta_b = -2\pi/3$ and $\theta_c = 2\pi/3$, respectively.

In this paper, the analysis is based on the in-phase disposition PWM (PDPWM). The reference signals and the carrier waveforms are shown in Fig. 3. According to the modulation principle of 3L-NPC-VSI, one fundamental period can be divided into six sectors $I-VI$ and each sector is further divided into A and B.

Assuming that the load is linear and ignoring the high frequency current harmonics of the inverter bridges, the three phase output phase current i_x are given by

$$i_x = I_m \cos(\theta + \theta_x - \varphi) \tag{5}$$

Where I_m is the current peak value, φ is the power angle of the inverter load.

Fig. 4 shows the detailed PWM waveforms over one carrier period during sector I-A and I-B for 3L-NPC-VSI. Table 1 present the procedures to derive the average and rms values of dc-link current for sector I-A and I-B. It should be noted that the average values expression $i_{up,ave}$ and $i_{down,ave}$ represent the average values over a carrier period, but the rms values expression $I_{up,rms}$ and $I_{down,rms}$ are calculated based on fundamental period.

Table 1 Dc-link current calculation for 3L-NPC-VSI over sector I-A and I-B

Sector	Modulated Duty Cycle	Active Duty Cycle	Current id	Id,ave	Id,rms
I-A	$\delta_{a1}=m\cos(\omega t),\ \delta_{a2}=0$	UP	i_a	$i_{up,ave}=mI_m\cos(\omega t)\cos(\omega t-\varphi)$	
	$\delta_{b1}=0,\ \delta_{b2}=-m\cos\left(\omega t-\frac{2\pi}{3}\right)$	DOWN	i_c	$i_{down,ave}=-\frac{1}{2}mI_m\left(2\cos\varphi-\cos(2\omega t-\varphi)\right)$	$I_{up,rms}=I_m\sqrt{\frac{\sqrt{3}}{4\pi}m\left(1+4\right.}$
			i_b+i_c		
I-B	$\delta_{c1}=0,\ \delta_{a1}=m\cos(\omega t),\ \delta_{a2}=0$	UP	i_a	$i_{up,ave}=\frac{1}{4}mI_m\left(\cos(2\omega t-\varphi)+4\cos\varphi-\sqrt{3}\sin(2\omega t-\varphi)\right)$	$I_{down,rms}=I_m\sqrt{\frac{\sqrt{3}}{4\pi}m\left(1+\right.}$
	$\delta_{b1}=m\cos\left(\omega t-\frac{2\pi}{3}\right),\ \delta_{b2}=0$	DOWN	i_a+i_b		
			i_c	$i_{down,ave}=-mI_m\sin\left(\omega t+\frac{\pi}{6}\right)\cos\left(\omega t-\varphi-\frac{\pi}{3}\right)$	

From table 1, the sum of the average current $i_{up,ave}$ and $i_{down,ave}$ is not zero, which cause the undesired low-frequency oscillation of the NP voltage.

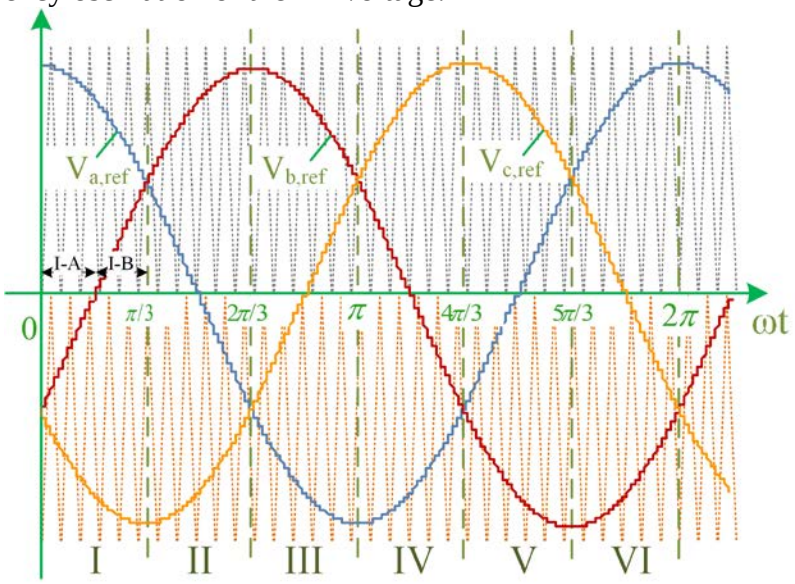

Fig. 3: Reference signals and carrier waveforms.

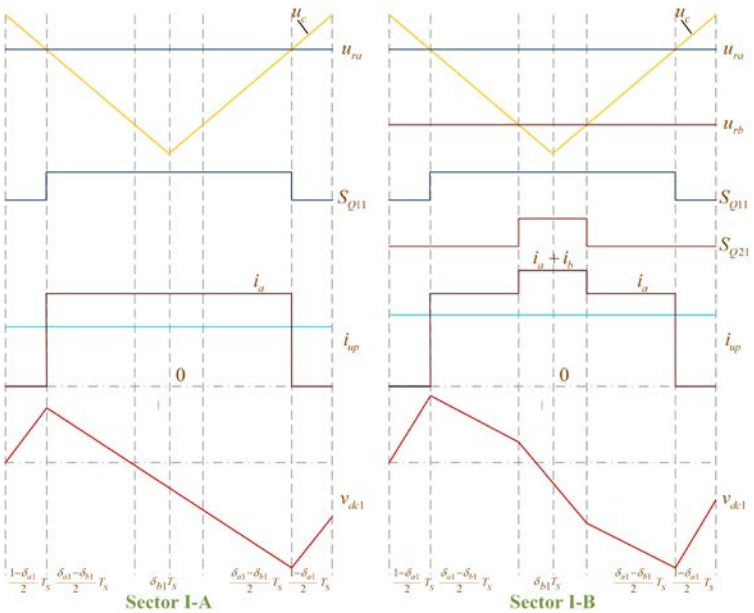

Fig. 4: Detailed PWM waveforms over sector I-A and I-B for 3L-NPC-VSI.

B. Modified SPWM for NP Voltage Control

In Fig. 1, the relation between $i_{up,ave}$ and $i_{down,ave}$ can be got from power equivalent relation as (6). Thus the NP voltage balancing equation can be expressed as (7).

$$i_{up,ave} - i_{\text{down},ave} = \frac{3}{2} m I_m \cos\varphi \tag{6}$$

$$i_{up,ave} = \frac{3}{4} m I_m \cos\varphi \tag{7}$$

Taking sector I-A as an example, the three-phase zero-sequence injected reference signals can be expressed as

$$v'_{x,ref} = v_{x,ref} + v_{zx} \tag{8}$$

where v_{zx} represent the injected zero-sequence signal. From (7), the NP voltage balancing equation is

$$\left[m\cos(\omega t) + v_{zx}\right] I_m \cos(\omega t - \varphi) = \frac{3}{4} m I_m \cos\varphi \tag{9}$$

$$v_{zx} = \frac{3m\cos\varphi/4}{\cos(\omega t - \varphi)} - m\cos(\omega t) \tag{10}$$

From (10), we get the widely used SVM based NP balancing strategy in [3] which uses the small vector for control. The main drawback of this approach is that the control authority over the NP current is limited. It is impossible to completely control the NP voltage when the modulation index m is high and for low power factors. The main reason for this is the existence of power angle φ in v_{zx}.

To completely control the NP voltage, here, taking the division of modified modulation signals into consideration.

$$v'_{x,ref} = v_{xp} + v_{xn} \tag{11}$$

Where $v_{xp} \geq 0$ and $v_{xn} \leq 0$. It's noted that the division of the signals will increase the switching frequency thus increase the switching loss. Also to obtain the maximum modulation index for the linear-modulation mode, we just divide the medium of the three-phase reference signal. Taking sector I-A as an example, from (7), the NP voltage balancing equation is

$$\left[m\cos(\omega t) + v_{zx}\right] I_m \cos(\omega t - \varphi) + v_{bp} I_m \cos\left(\omega t - \frac{2\pi}{3} - \varphi\right) = \frac{3}{4} m I_m \cos\varphi \tag{12}$$

By dividing power factor φ from (ωt - φ), the derived modulation signals are

$$v_{zx} = -\frac{m\cos(\omega t) + m\cos(\omega t + 2\pi/3)}{2}, v_{bp} = \sqrt{3}/2 \times m\sin(\omega t), v_{bn} = -\sqrt{3}/2 \times m\cos(\omega t + \pi/6) \tag{13}$$

Expression (13) shows the carrier based nearest three virtual space vector PWM in [6]. It can make the maximum modulation index to 1.15 at the expense of increasing the switching loss. Further solution can be found for (8) but not necessary for the consideration of maximum modulation index and switching loss.

C. RMS Value of DC-Link Current

From Table 1, the rms dc-link currents of 3L-NPC with traditional PDPWM are

$$I_{up,rms} = I_{up,rms} = I_m \sqrt{\frac{\sqrt{3}}{4} m\left(1 + 4\cos^2\varphi\right)} \tag{14}$$

Expression (14) can be extended to any other PDPWM. Taking sector I as an example for deviation. The rms dc-link current of average dc-Link current based NP voltage balancing algorithm are

$$I_{\text{up},rms} + I_{down,\text{rms}} = \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left[i_a^2\left(v'_{a,ref} - v'_{bp}\right) + i_c^2 v'_{bp} + i_c^2\left(-v'_{c,ref} + v'_{bn}\right) + i_a^2\left(-v'_{bn}\right)\right] d\theta = \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left[i_a^2\left(v'_{a,ref} - v'_{b,ref}\right) + i_c^2\left(v'_{b,ref} - v'_{c,ref}\right)\right] d\theta \tag{15}$$

Due to the symmetrical operation of the inverter, $I_{up,rms}$ and $I_{down,rms}$ got the same expression shown in (14).Thus the rms values of the capacitor current $I_{C,rms}$ is calculated as

$$I_{\text{C},rms} = \sqrt{I_{up,ave}^2 - I_{up,rms}^2} = I_m \sqrt{\frac{m}{2}\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8} m\right)\cos^2\varphi\right]} \tag{16}$$

Comparison of DC-Link Performances and Simulation Results

The comparison is based on the conditions that the NP balancing problem have been solved by modulation. Since the dc-link capacitor voltage ripple in 3L-NPC-VSI and 2L-VSI are significantly related to the modulation strategy. Take the case that 2L-VSI uses SVM and 3L-NPC-VSI uses the carrier based nearest three virtual space vector PWM shown in (13), the results are shown in table 2.

Table 2 Comparison of dc-link performs between 2L-VSI and 3L-NPC-VSI

Topology	Id,ave	Id,rms	vp,rip	vmax,m	vmax,pf
3L-NPC	$i_{up,ave}=\frac{3}{4}mI_m\cos\varphi$	$i_{up,rms}=I_m\sqrt{\frac{\sqrt{3}}{4\pi}m\left(1+4\cos^2\varphi\right)}$	$\left\|v_{c,rip}\right\|_{max}=\frac{I_mT_s}{8C_{dc}}$	$\frac{2}{3}$	1
2L-VSI	$i_{d,ave}=\frac{3}{4}mI_m\cos\varphi$	$i_{d,rms}=I_m\sqrt{\frac{\sqrt{3}}{4\pi}m\left(1+4\cos^2\varphi\right)}$	$\left\|v_{c,rip}\right\|_{max}=\frac{I_mT_s}{8C_{dc}}$	$\frac{2}{3}$	1

From table 2, the dc-link characteristics for both topologies are similar if both are controlled without low-frequency oscillation. It should be noted that C_{dc} in table 2 refers to the total dc-link capacitor.

Fig. 5 shows the simulation parameters for 2L-VSI and 3L-NPC-VSI. It can be seen that the capacitor voltage consists of double carrier frequency harmonics for 2L-VSI and carrier frequency for 3L-NPC-VSI.

Rated Power (Pn/kVA)	80
Rated Voltage (Vn/V)	380
Rated Frequency (fn/Hz)	50
Switching Frequency (fs/Hz)	5.4k
DC-Link Capacitance (Cdc/μF)	2400
Filter Inductance (Lf/μH)	112
Filter capacitance (Cf/μF)	1200
Resistance Load (R_load/Ω)	1.8

Fig. 5: Simulation parameters

Fig. 6 and Fig. 7 show that the voltage ripple magnitudes are 1.1V for 2L-VSI and 1.0V for 3L-VSI with modulation index at 2/3, which are identical with table 2. Therefore, the analytical results above can be used for the dc-link capacitor design.

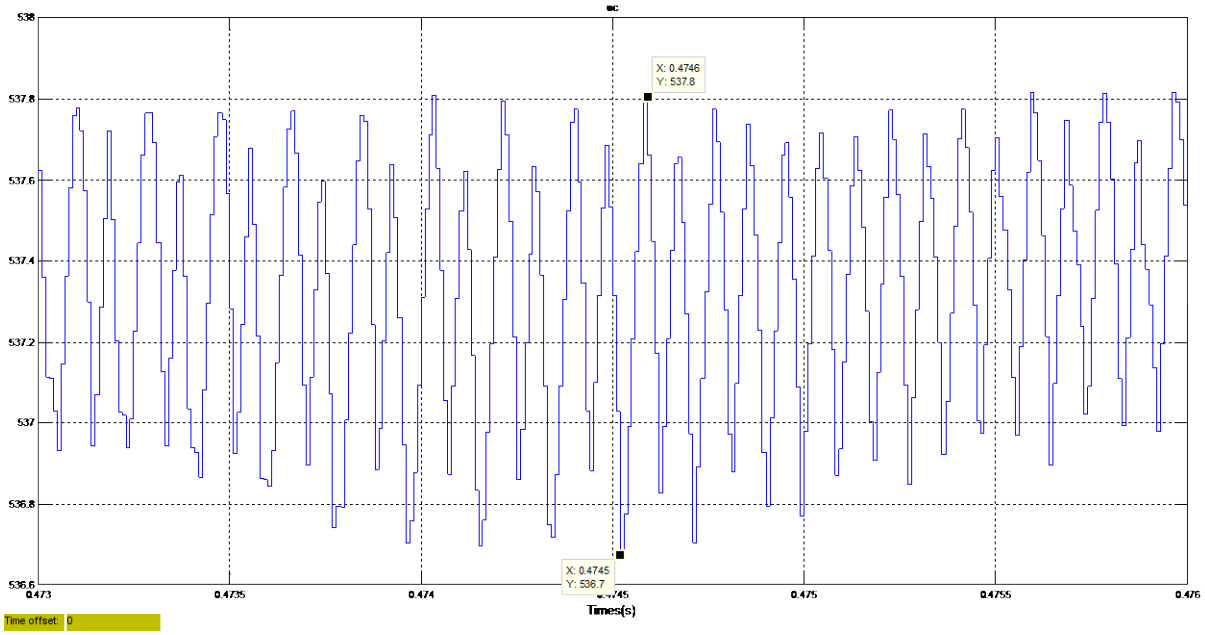

Fig. 6: Voltage ripple for 2L-VSI

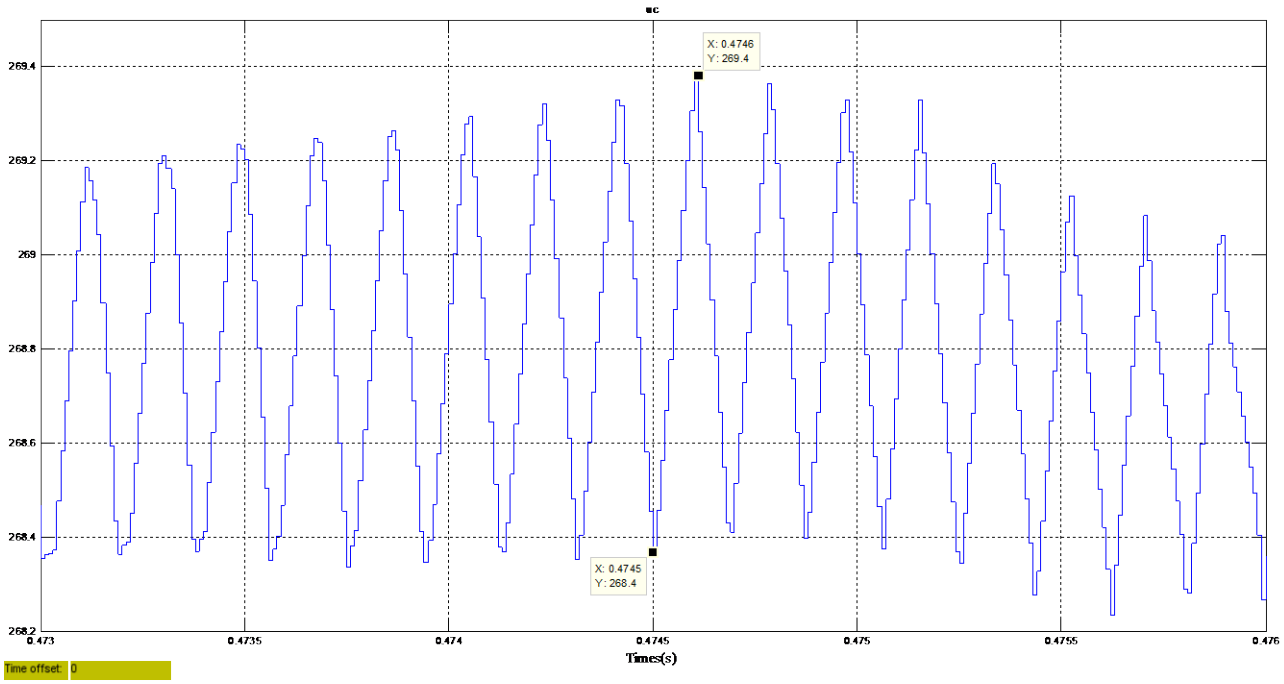

Fig. 7: Voltage ripple for 3L-NPC-VSI

Conclusions

We give a general analytical calculation of dc-link current and voltage ripple for three-level three-phase neutral-point-clamped voltage source inverter (3L-NPC-VSI). The general expression of the root-mean-square (RMS) dc-link current is derived. The performances of the 3L-NPC-VSI are demonstrated and compared with those of the 2L-VSI from the viewpoint of the dc-link average current, rms current, and voltage ripple. Simulation results validates the theoretical analysis. Therefore, the analytical results can be used for the dc-link capacitor design.

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