Design of novel full adder based on resonant tunneling diode

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Abstract. The resonant tunneling diode (RTD) has attracted much attention because of its unique negative differential resistance (NDR) characteristic, RTD increases the powerful logic function of a single gate and is more suitable to implement the threshold gates. Recently, the generalized threshold gate (GTG) and the multi-threshold threshold gate (MTTG) have been proposed, which provide the more based circuit structures of RTDs. Meanwhile, the RTD full adder circuits with GTG and MTTG circuit structures have been proposed. In this paper, a novel full adder circuit based on RTD is proposed, compare to previous designs, the novel proposed circuit has better performance, which uses fewer devices and reduces 3.6%–11.5% power.

Introduction

As the most mature type of the quantum devices, the resonant tunneling diode (RTD) has better performance and features, such as self-latching, low-power, functional versatility, negative differential resistance characteristic (NDR), high speed, and so on. Due to the NDR characteristic of the RTD, RTD can be exploited to extend the functionality of a single gate [1,2]. Nowadays, the RTD is widely used in the low-power and high speed circuits [3-5].

The monostable-bistable logic element (MOBILE) is a basic logic block in circuit design of RTDs, as shown in Fig. 1(a). The MOBILE consists of two RTDs connected in series, the below one as driver device and the above one as load device which is driven by a switching bias voltage V_{clk}. When the V_{clk} is low, both RTDs in low resistance state, the MOBILE only has one steady state point S_0, as shown in Fig. 1(b), this state is called the monostable. When the V_{clk} increases to the threshold value $V_{SW} = 0.5V$, the RTD with smaller peak current will switch from low resistance state into high resistance state, the MOBILE will appear two steady state points S_1 and S_2, as shown in Fig. 1 (c), this state is called the bistable. Output is depended on the RTD which has a smaller peak current. If the load RTD has a smaller peak current, the output will become stable at S_1 and the $V_{out} = 0$. Otherwise, the output will switch to S_2 and the $V_{out} = 1$[6]. To increase the functionality of the RTD circuit, the multi-threshold threshold gate (MTTG) [7] and the generalized threshold gate (GTG) [8] have been proposed. The MTTG can realize various threshold by extending the conception of MOBILE to a series connection of three or more RTDs. The GTG can implemented different logic functions by using the transistor network instead of a single heterostructure field-effect transistor (HFET) to control input branches.The threshold structure as shown in Fig.1 (d) [9].

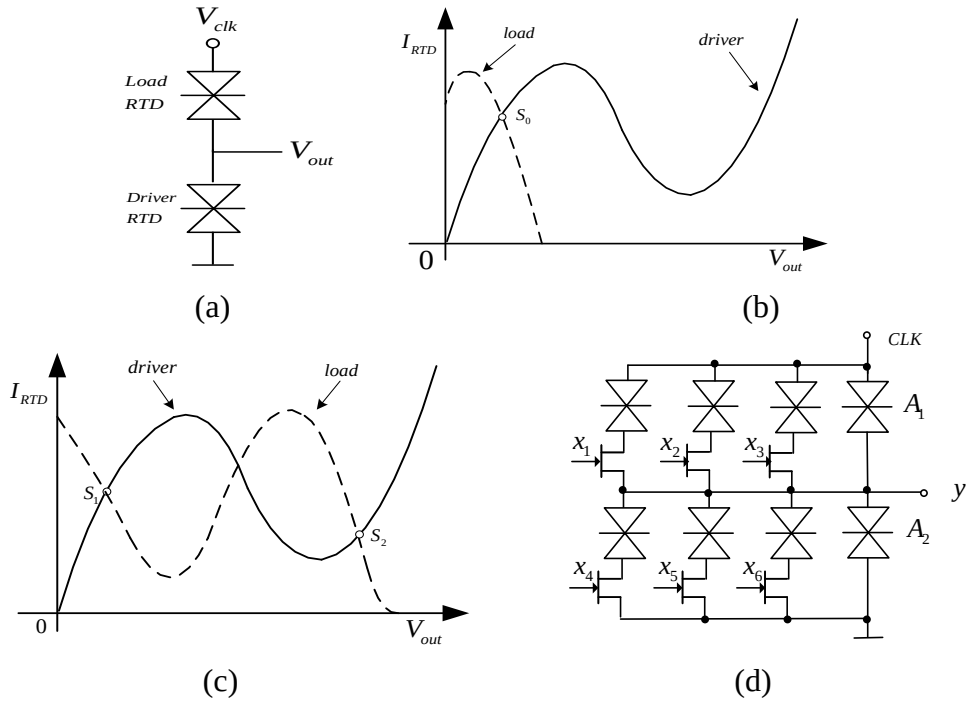


Fig.1: MOBILE (a) basic circuit (b) monostable (c) bistable (d) threshold gate structure

Full adder is the fundamental arithmetic element that decides the overall performance of the circuits and is widely used in many very large-scale integration (VLSI) systems [10]. The RTD full adder circuit already has been proposed [11-13], but the circuit is relative complex. In this paper, we propose a novel full adder circuit based on RTD and simulate the result by HSPICE. This novel RTD full adder has better performance in power and delay.

Previous designs

One of the basic circuit structures based on RTD is the threshold gate (TG) structure, the TG is a logic gate which has n binary input variables and an binary output variable. Its internal parameters are as follows: a set of n positive or negative weights, $\{w_i\}(i=1,2,...,n)$, and a threshold T, such that its input-output relationship is [14]

$$y=\begin{cases}1, & if \sum_{i=1}^{n} w_i x_i \geq T \\ 0, & otherwise\end{cases} \tag{1}$$

The Eqs. (1) can also be presented as $f=<w_1x_1+...+w_nx_n>_T$. If a logic function can be implemented by a single threshold logic gate, the logic function is called a threshold function. Otherwise, it is called a non-threshold function [14].

The full adder function can be described as follows: the addition of two inputs A and B with forestage carry C_{in} calculates the two outputs Sum and C_{out}, the Karnaugh map of Sum and C_{out} as shown in Fig.2 (a) and Fig.2 (b).

x_1 \ x_2x_3	00	01	11	10
0	1	1	0	1
1	1	0	0	0

(a)

x_1 \ x_2x_3	00	01	11	10
0	1	1	0	1
1	1	0	0	0

(b)

Fig.2: the Karnaugh map (a) Sum (b) C_{out}

The C_{out} is a threshold function, it can be realized by a single TG, it can be expressed as:

$$C_{out}=\begin{cases}1, & A+B+C_{in}\geq 2\\ 0, & otherwise\end{cases} \tag{2}$$

The Sum is a non-threshold function, it can't be realized by a single TG, rewrite the Sum as[13]

$$Sum=C_{out}\oplus f_M \tag{3}$$

where the f_M is a middle function, and defined as

$$f_M=\begin{cases}1, & 1\leq A+B+C_{in}<3\\ 0, & otherwise\end{cases} \tag{4}$$

Using the GTG structure to implement the f_M, it can be expressed as

$$f_M=(A+B+C_{in})\cdot\overline{ABC_{in}} \tag{5}$$

Two transistor networks of input branches are used to realize the functions $A+B+C_{in}$ and ABC_{in}.The full adder circuit (FA_GG) as shown in Fig. 3[13].

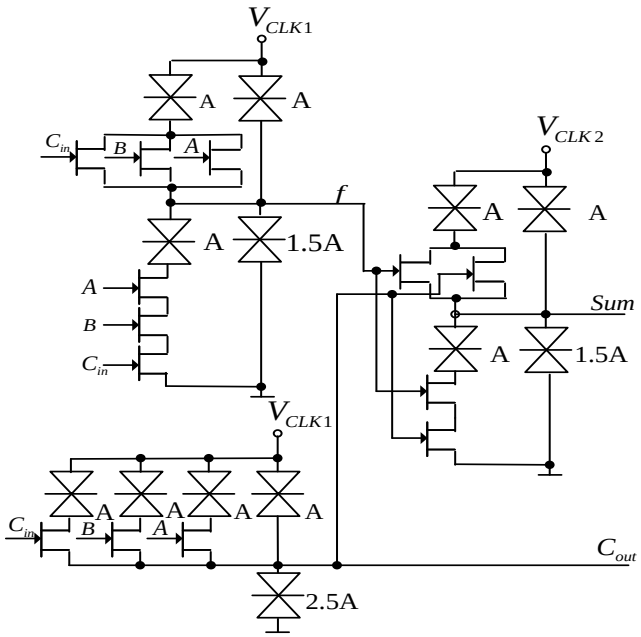
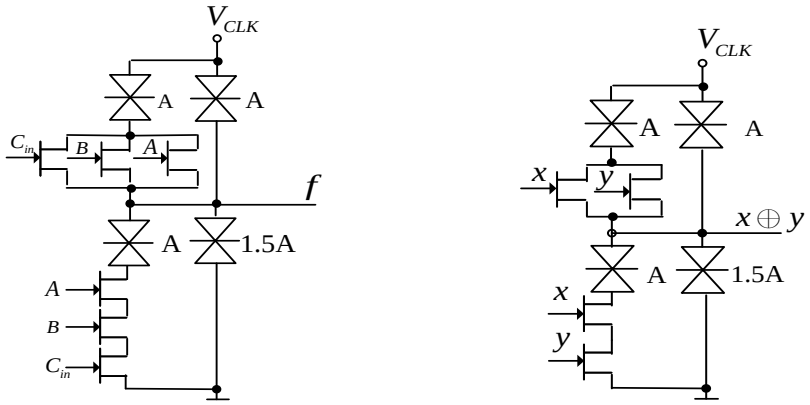


Fig.3: the full adder circuit (FA_GG)[13]

Novel full adder

To design fewer gates in full adder based on RTD, we analyze the Sum function, $Sum=A\oplus B\oplus C_{in}$, in literature [13], use the middle function to implement it by f_M_GTG and XOR_GTG, as shown is Fig. 4 (a) and Fig. 4 (b).



(a) (b)

Fig.4: RTD circuit (a) f_M_GTG (b) XOR_GTG

The RTD full adder circuit [13] should use the C_{out} as the input variable to produce the Sum, it will increase the delay, in order to reduce the delay, we directly implement the Sum function. Based on XOR_GTG, we design the RTD three-variable XOR gate to implement the Sum, as shown in Fig. 5.

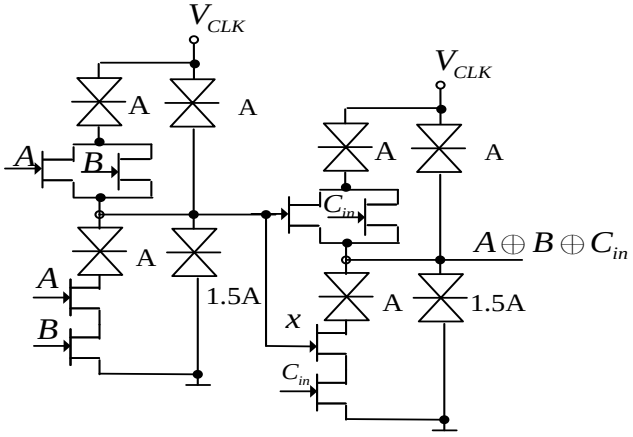


Fig. 5: RTD three-variable XOR gate

The full adder circuit can just use one stage to produce the result, as shown in Fig. 6. Compare to previous designs, we use 24 devices less than them.

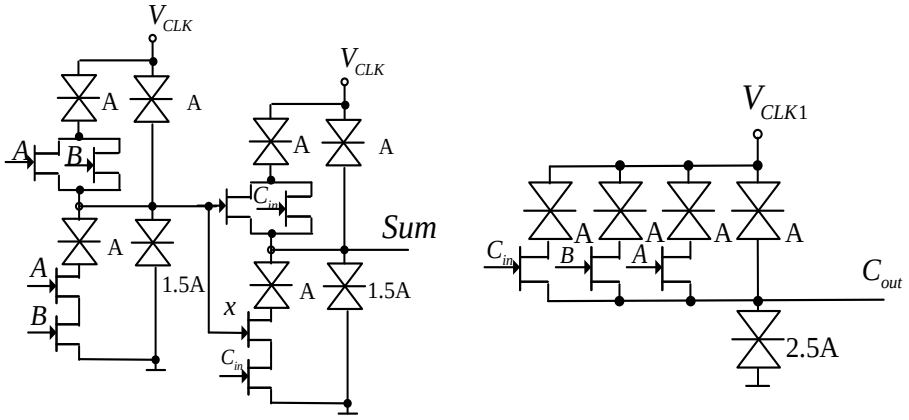


Fig.6: proposed RTD full adder

Simulation results

To test the performance of the proposed designs, the circuits are verified by HSPICE. The RTD model is consisted of three parts: a controlled current source in parallel a capacitor, and the whole part in series with a resistor [15]. The RTD parameters are set as follows: the capacitance is 4 $fF/\mu m^2$, the peak current density is 9 kA/cm^2, the peak voltage is 0.28 V, and the unit area A is 2 μm^2 [15]. The HFET is a depletion-type transistor with threshold voltage -0.1 V [4]. The conventional inverters in RTD full adder are designed with a TSMC 180 nm technology. Fig. 7 shows the simulation waveform of the designs, proposed circuit and FA_GG, at the frequency of 1 GHz. By observing the waveform can get the result is correct.

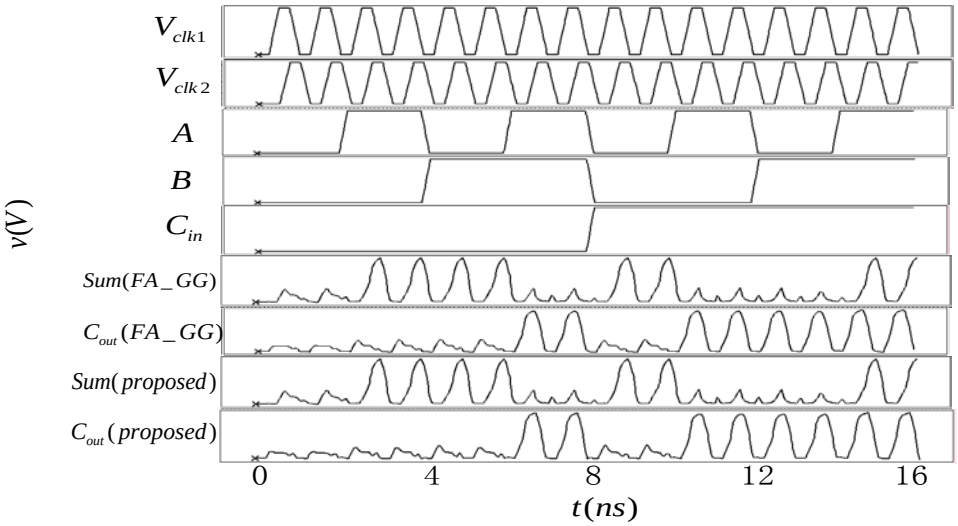


Fig. 7: HSPICE simulation waveform for FA_GG and proposed circuit

The power of FA_GG and proposed circuit in different working frequency as shown in Table 1. The results indicate the proposed circuit has better performance, which reduces 3.6% – 11.5% less power than FA_GG.

Table 1: the power of FA_GG and proposed circuit in different working frequency

Frequency(MHz)	500	750	1000	1500
Designs	Power(μW)	Power(μW)	Power(μW)	Power(μW)
FA_GG	99.7	104.4	116.3	122.3
Proposed	96.1	97.7	102.9	109.6

Conclusion

In this paper, a novel RTD full adder circuit has been proposed, which is composed of a three-input C_{out} gate and a three-variable XOR gate. From the simulation results, the proposed circuit has the correct logic function. Compare to the FA_GG, the proposed circuit has better performance, it uses 24 devices less than FA_GG which uses 26 devices. Meanwhile, the proposed circuit just use one stage to produce the result that it has fewer power-delay product, and it reduces 3.6%-11.5% power compared with the FA_GG. Hence, the proposed RTD full adder circuit provides a better circuit for RTD circuit designs.

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