

Dual Redundant Flight Control System Design for Microminiature UAV

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Abstract. The rigorous requirement for safety, reliability, maintainability, and miniaturization in microminiature unmanned aerial vehicle (UAV) has motivated significant research in new technology. A dual redundant fault-tolerant flight control platform is designed based on the technology of system on a programmable chip (SOPC) and fault tolerance. The scheme of fault-tolerant system is carried out in detail from both hardware and software perspectives. The key technology of the synchronization, fault diagnosis and location, dynamic reconfiguration and isolation is studied in detail. After lots of simulations and experiments, it indicates that the design is reasonable. The platform not only realizes the basic function of the flight control, but also has a high level of integration and flexibility, and can keep safe after a failure.

Introduction

With the development of aviation microelectronics, micro sensors and control theory technology, microminiature unmanned aircraft vehicle (UAV) which has small size, flexible application, strong concealment and low power consumption has been widely used in civil and military field. As microminiature UAV application scope expands, the complexity of task execution increases and the environmental condition is variable and complex. Therefore, the requirements of reliability and stability of the UAV is higher and higher.

Flight control computer is the core part of UAV flight control system. Its typical application functions include reading and processing sensors data, performing control law computations, sending commands to actuators, management of the navigation control and radio link and so on. So its reliability and safety is directly related to the performance of the UAV [1]. To improve the dependability of flight control computer, it is difficult to meet the requirement only from aspects of the quality of components or assembly process. Whereas, the architecture of the flight control computer is key to the property. Hence, the better choice is to use redundant fault-tolerant techniques to improve the system reliability, guarantee the flight stability and safety of UAV and complete all kinds of complicated task.

Nevertheless, fault-tolerant design of flight control computer will bring the redundancy of system structure. It is also necessary to design a fault-tolerant flight control platform that could satisfy the requirement of miniaturization.

Fault-tolerant System Design

In design of fault-tolerant flight control system structure, the selection of redundancy scheme and model is the key. Generally, fault-tolerance is achieved through modular redundancy and the voting of data from replicated tasks based on hardware, software and time.

The Redundancy Structure of System. The redundancy technology can improve the mission reliability of flight control computer system, but system task reliability is not proportional to the redundancy number. Because along with the increase in redundancy number, the corresponding devices with functions include detection, judgment and arbitration, isolation and switching are bound to increase. Their basic reliability in series will decrease the overall system reliability. Therefore, the choice of the redundancy number should be from the perspective of overall system

dependability, and take the size, weight, cost and redundancy management manner into account. Duplex redundant flight control computer system has small dimension, light weight, low cost and fine electromagnetic compatibility. It is a preferred choice for microminiature UAV.

According to different standard, redundant structure has different classification. In a dual redundant system, there are three types by working pattern of the redundant part: standby reserve type, load sharing redundant type and double machine parallel redundant. Double machine parallel redundant type not only satisfies the real-time and reliable requirement of flight control system, but also will not lead to reset after failure. It can avoid blind area of control in time, and realize the seamless switching of two machines [2]. Microminiature UAV usually has small size and high integration, but modular redundancy design will make the system size and power consumption multiplied. Considering the central processing unit (CPU) is the "brain" of flight control system platform which plays a key role, and the hardware usually has a better stability than software, this design is only to focus on the design of processor redundancy.

Reliability of Dual Redundant System Analysis. The flight control computer hardware malfunction is mainly caused by fault of the key device which belongs to the accidental failure at large. The actual reliability function is close to exponential function. For the reliability function of the uniprocessor

$$R_S(t) = e^{-\lambda t} \quad (1)$$

Type: λ is system failure rate (unit is 1/h); t is the unit work time (unit is h).

Dual redundant flight control computer is two single redundant units (single machine) in parallel, so its reliability

$$\begin{aligned} R_{DMR}(t) &= C_2^2 R_S^2 + C_2^1 R_S(1 - R_S) \\ &= 2e^{-\lambda t} - e^{-2\lambda t} \end{aligned} \quad (2)$$

Mean time to failure of system (MTTF) is the expectation of the first failure time. It can be calculated by the probability density function. The MTTF of single and double machine system can be calculated respectively.

$$T_{M,S} = \int_0^{\infty} R_S(t) dt = \frac{1}{\lambda} \quad (3)$$

$$T_{M,D} = \int_0^{\infty} R_{DMR}(t) dt = \frac{3}{2\lambda} \quad (4)$$

It is obvious that the MTTF of dual redundant system is longer than the single's by the deduction of Eq. 3 and Eq. 4. That is, the probability of breakdown is smaller. Thus, the reliability of flight control system is greatly improved through using double redundancy technology.

Dual Redundancy System Management. Redundancy management is a key point in the redundancy design. It is in charge of the management of redundant system running mechanism and malfunction handling. Its purpose is to maximize system resource utilization, enhance the flexibility of the system dynamic reconfiguration and make the system have great fault-tolerance. In a duplex redundant fault-tolerant system, one is a host machine and the other is vice. Both of them complete the same tasks at the same time, communicating and supervising each other at predefined intervals. When the malfunctions happen, the arbitration module selects and switches the output channel [3]. The working block diagram is illustrated in Fig. 1.

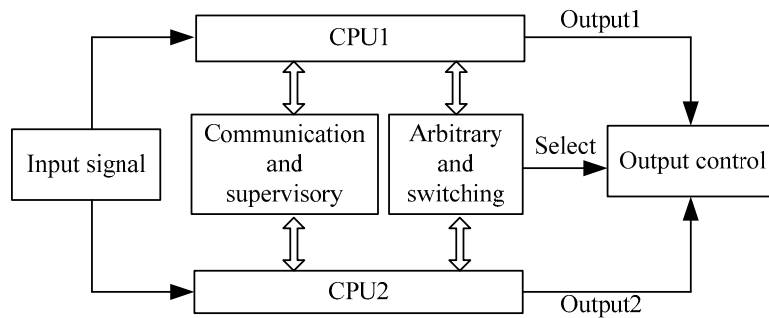


Fig. 1 Double redundant fault-tolerant system block diagram

Flight Control Platform Design

System Platform Composition. Microminiature UAV must have higher integration and lower power consumption as much as possible because of its own characteristics. It is crucial to choose an appropriate development platform. The system on a programmable chip (SOPC) with flexible design, high integration, and low power consumption has the programmable software and hardware. If the SOPC technology is applied to microminiature UAV flight control computer, it not only can further realize the miniaturization of UAV, but also can improve the flexibility of design and easy upgrade.

The CPU of flight control system platform is the field programmable gate array (FPGA) of Altera Company's Cyclone IV series with high performance and low power consumption. The external circuits include storage module, signal conditioning module, A/D and D/A module, communication module, interface module et al. The system block diagram is shown in Fig. 2.

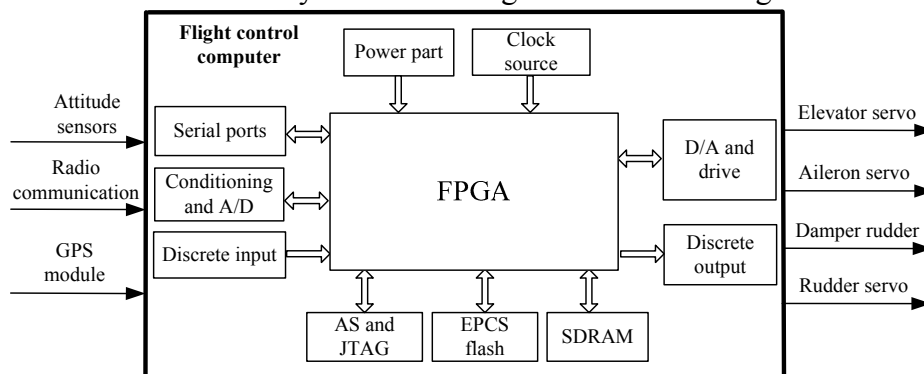


Fig. 2 The system hardware block diagram

The sensor module of UAV collects analog signal includes height, velocity, and attitude et al. Then it will be converted into digital signal after filtering. The processor will use the digital signal to calculate output control signal by the control law of the aircraft. The output control signal will drive steering gear after D/A module converting it into analog signal. The UAV is to accomplish the flight attitude adjustment through adjusting the corresponding control surface by the servo [4].

Dual-core Design in FPGA. In the signal FPGA chip processor, there are two Nios IIs embedded to compose a duplex redundant system structure to improve the system fault-tolerant ability and enhance the system reliability. The driver of A/D, D/A conversion module, RS232, RS422, and CAN periphery module is written in Verilog language, and then encapsulated as IP cores mounted to the Nios II Avalon bus. So the processor can communicate with peripheral devices at any time with high efficiency. Due to the communication of peripheral modules is realized by IP core in hardware, it is more real-time and stable than in software. The design of FPGA internal system structure is illustrated in Fig. 3.

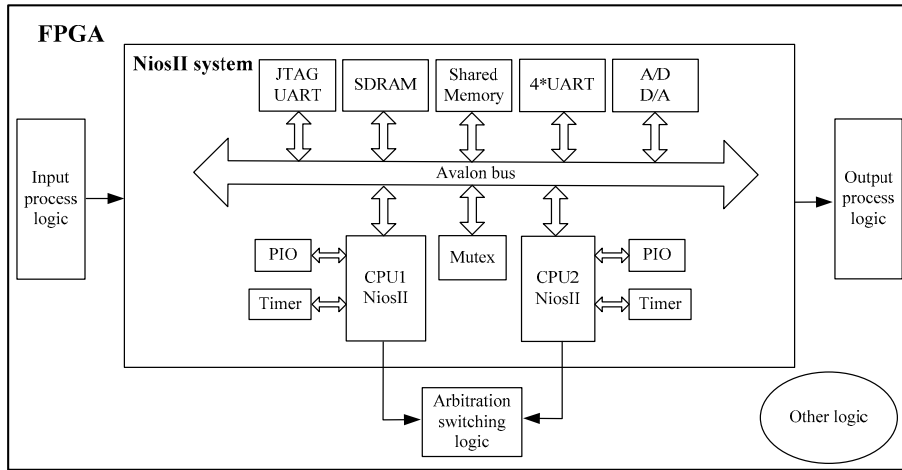


Fig. 3 FPGA internal system structure

The Task Design of Redundancy System. The software development of flight control system is mainly the development of FPGA. The driver of peripheral modules is written by Verilog and encapsulated into IP cores. Integrate dual-core processor and IP components in the internal structures of FPGA by Qsys tool. Finally, develop and program software of CPU1 and CPU2 using the NiosII EDS software, respectively. In order to accommodate common-mode faults and improve the system reliability, one software program is in C language and the other uses assembly language.

Dual redundant fault-tolerant system consists of two processors which respectively finish sensor signal collecting and processing, calculation of flight control law, ground station communication, fault self-diagnosis, and test tasks. Dual-core resource sharing, mutual communication and supervision are implemented by a Mutex. According to the management of fault information, the aircraft would output correct control signal to finish safe flight with a failure. The system software architecture is illustrated in Fig. 4.

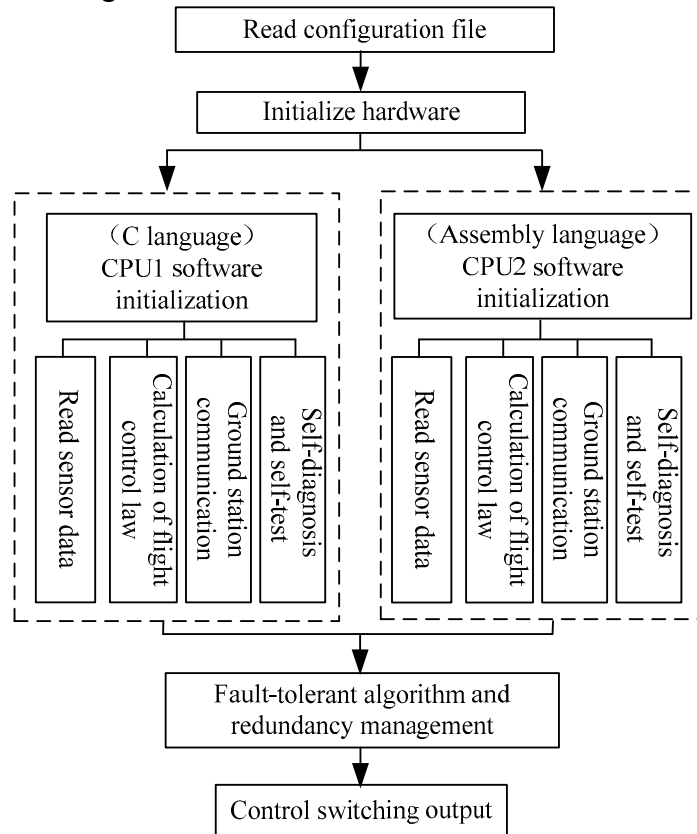


Fig. 4 Non-similar redundant software architecture diagram

Key Technology Research in Fault-tolerant System

Synchronization and Communication. Synchronization is the basic core of redundancy management. It is meaningful to compare and vote for the fault-tolerant system only when redundancy modules act in unison. The synchronization generally can be classified as clock synchronization, loose synchronization, and task synchronization. Among them, the task level synchronization has loose execution, no clock synchronization, and very high real-time and flexible operation. It is based on an independent operation with certain logic as the synchronization foundation. And it sets up one or more comparing points in the task to judge consistency at predefined intervals [5]. Double machine task synchronization process is shown in Fig. 5.

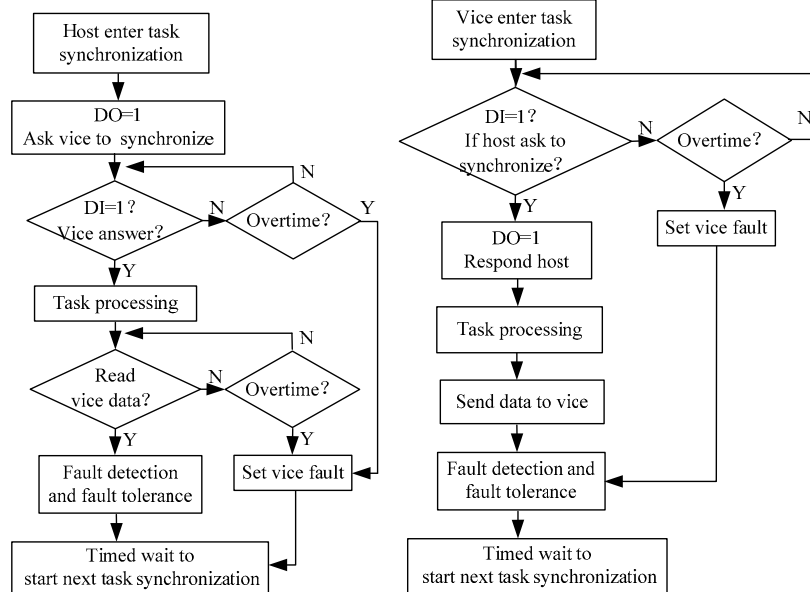


Fig. 5 Dual-task synchronization flowchart

Fault Diagnosis and Localization. Fault diagnosis and localization mainly depend on mutual check and self-inspection of the dual machine. The mutual inspection is to compare inputs, intermediate operation results and outputs to vote in real time. The host reads the vice machine data to compare at predefined intervals. If the corresponding data is inconsistent, there is at least one fault machine. So host and vice machine start to self-check and self-test to verdict. Concrete implementation methods are:

- 1) Detect the sensor interfaces to check validity such as checking range, slew rate to avoid abrupt faults, mean or RMS to avoid incipient faults.
- 2) Set the timer supervision (commonly known as "watchdog"). Execute updating data register in a regular time in software running. If program runs away or runs into an endless loop, the timer set output from "1" to "0" to report failure.
- 3) Detect A/D and D/A module by loading fixed voltages to test. If the comparison results are outside of range of allowable error, it breaks down.
- 4) Run calculation program with a known result and compare the result with the predefined result. If there is a discrepancy between the two, the processor has failure.
- 5) Read the pre-stored data in sharing on-chip RAM. If the acquisition of Mutex or reading RAM has problems, the data could not read within the preset time or discord. That is, the processor is off normal.

Dynamic Reconfiguration. After fault diagnosis, arbitration logic would select fine processor to control the output according to fault signal and the priority. When two processors are normal, the prior is the host to control output [6]. After the host fails, the vice (low priority) is to replace the host and run into a stand-alone mode. The logic of enable signal of control output:

$$Out_sel = Pr \cdot Ao + \overline{Pr} \cdot Ao \cdot \overline{Bo} \quad (5)$$

Wherein, “Pr” is the processor priority signal, "1" represents a high priority, "0" indicates a lower priority. “Ao” and “Bo” represent a fault signal of processors A and B, "1" indicates that the processor is intact, "0" is defective.

Dual-processor Output Switching Verification

In order to ensure the redundancy management module can correctly finish arbitration logic and channel switching according to the fault information. The simulation result of output channel switching in Fig. 6 was artificially injected fault information. Among them, the “Pr_A” and “Pr_B” are respectively the priority signal of processor A and B. The priority of A is higher than B’s. “Ao” and “Bo” are respectively A and B fault signal, "0" is the fault. “Out_sel” is select signal of output control. The "1" indicates that processor A acts as the host to control output, while "0" is B to act as host. According to the injection fault signal, channel selection is correct and the fault isolation and system reconfiguration can realize.

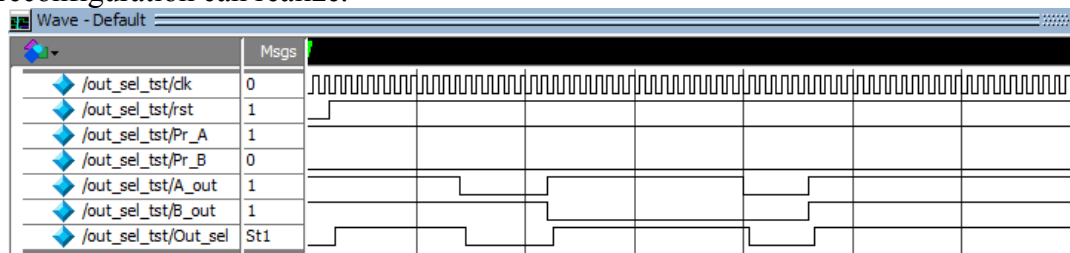


Fig. 6. Channel switching waveform simulation

Summary

Combining the SOPC and fault-tolerant technology in the design of microminiature UAV flight control platform, this paper gives a particular analysis and design from hardware and software. By simulation and practical test, this scheme not only can finish flight, but also can realize fault detection, isolation and system reconfiguration. Practice proves that this design can effectively solve the problem of microminiature UAV which has contradiction between small size, light weight, and high integration with high reliability. This design improves the reliability, availability, maintainability and safety of flight control computer. It has a broad application prospect.

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References

- [1] Zolghadri A, Henry D, Cieslak J, et al. Fault Diagnosis and Fault-Tolerant Control and Guidance for Aerospace Vehicles. Springer London [M], 2014: 119-149.
- [2] L-F. Yang. Unmanned aerial vehicle fault tolerant flight control systems research [D]. Nanjing: Nanjing University of Aeronautics and Astronautics, 2007.
- [3] C. Jun, S. Nan, and G-Z. Xiong “Design and implementation of a fault-tolerance real-time computer architecture,” Journal of University of Electronic Science and Technology of China, vol. 36, no. 5, pp. 846–849, Oct.2007.
- [4] Efimovs D, Cieslak J, Henry D. Supervisory fault-tolerant control with mutual performance optimization [J]. International Journal of Adaptive Control and Signal Processing, 2013, 27(4): 51-279.
- [5] Patton, Ron J. "Fault-tolerant control systems: The 1997 situation." IFAC symposium on fault

detection supervision and safety for technical processes. Vol. 3. 1997.

[6] Q.-Z. Zhou, et al. Fault Tolerant Reconfigurable System with Dual Module Redundancy and Dynamic Reconfiguration [J]. Journal of Electronic Science and Technology, 2011, 9(2): 167-173.