Principle and Realization for Simulated Speed Sensor of High-speed Rail

Li Guoda

Beijing institute of technology School of Information and Electronics, Beijing,100070, China

lcdspider@163.com

Keywords: DDS, simulative speed sensor, FPGA, serial port communication.

Abstract. In order to test the function of the SDU module in the static environment, we design the simulative speed sensor by studying the principle of the speed sensor. We confirm the function requirements and the parameter of the simulative speed sensor by testing the speed sensor. According to the requirements, a DDS scheme based on FPGA is designed as the core of the simulative speed sensor. With the DDS scheme and the related circuit, the function of the simulative speed sensor has been approached.

Introduction

With the gradual development of high-speed rail in China, the control equipment of high-speed rail has already produced in large-scale and successively put into use, ATP, as the vehicle part of control equipment for high-speed rail, how to conveniently and better commission and detect ATP and guarantee its quality and normal function has become to be one important problem.

SDU module is the sub-module of ATP, it is responsible for receiving speed signal of speed sensor in the operation process of high-speed rail, and it converts into digital signal to feed back to ATP to control train. Because SDU module is responsible for providing data involves with safety for running speed of rail, once module is ineffective it will cause serious consequence, therefore, how to make functional detection on SDU in production and daily maintenance period has become to be one problem urgently needs solution.

Work principle of 2-phase speed sensor used by high-speed rail

Work principle of 2-phase speed sensor.

At present, ATP uses 2-phase speed sensor of MiniCoder GEL 247, this one is based on Hall Effect and driven by DC power of 10V to 30V, it can produce square signal with 2-phase difference of 90 degree and frequency of 0-25khz.

Electrical data	
supply voltage	U_B = 10 ... 30 V DC, reverse polarity protected
current consumption without load	$I_B \leq 60$ mA; $I_B \leq 30$ mA (with frequency divider)
output signals	square-wave, push-pull driver I_{max} = 20 mA
input and output frequency	0 ... 25 kHz

Diagram 1 Index of sped sensor

Diagram 2 Speed sensor

Connection between SDU and speed sensor.

SDU module has 2 signal channel, they are respectively connected with 2 signals of 2-phase speed sensor, of which, V_+ and V_-provides DC power of 18V used by 2-phase speed sensor, S is used to receive speed signal sent by speed sensor. It is indicated by the following diagram:

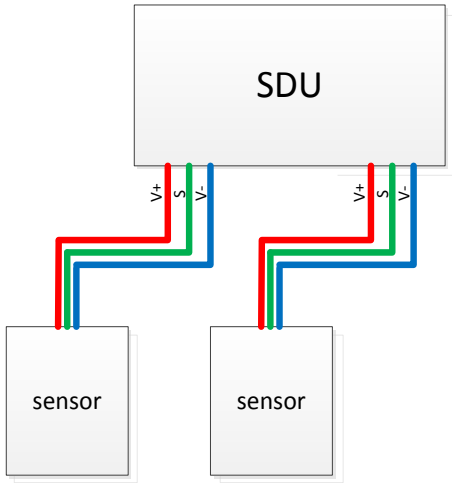

Diagram 3 SDU and speed sensor

Actual work data of speed sensor.

If we want to simulate functions of speed sensor, we need also to learn signal wave form in actual work environment generated by speed sensor as well as relations between signal frequency and rail speed. This needs to make measurement and analysis on speed sensor signal in actual running environment of rail.

1) Connection of test equipment

Respectively connect positive of channel 1 of OSC into S, V signal of the first signal of SDU, the positive of channel 2 is respectively connected into S, V signal of the second channel of SDU. It is indicated by the following diagram:

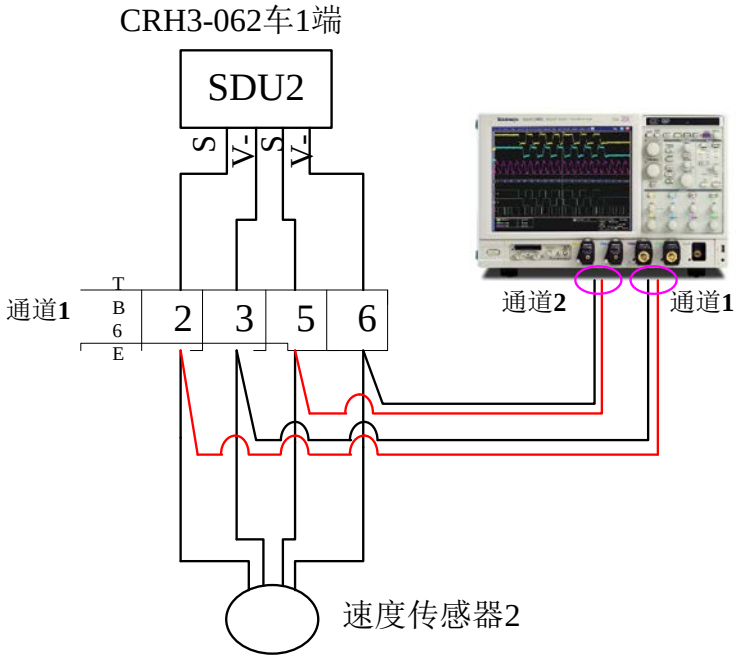

Diagram 4 Indication diagram for connection of test equipment

2)Test methods

Record wave forms of speed sensor by OSC when rail is running at the speed of 50km/h, 100km/h, 200km/h and constant speed of 300km/h, meanwhile the testers are record speed value of DMI, GPS and rail.

In the test process, rail is kept in different speed for certain time so as to reach complete data record. The detailed methods are indicated by the following table:

Table 1 Test steps

Step	Operation
1	Make rail speed up to 50km/h and maintains 10s, store wave form information of OSC, meanwhile record DMI, GPS and rail speed at this time.
2	Make rail speed up to 100km/h and maintains 10s, store wave form information of OSC, meanwhile record DMI, GPS and rail speed at this time.
3	Make rail speed up to 200km/h and maintains 10s, store wave form information of OSC, meanwhile record DMI, GPS and rail speed at this time.
4	Make rail speed up to 300km/h and maintains 20s, store wave form information of OSC, meanwhile record DMI, GPS and rail speed at this time.

3)Test data and analysis

Wave form and some print-screen of speed sensor 1 collected by OSC are indicated by the following diagram:

Diagram 5 Wave form output by speed sensor

Test data

Extract signal, frequency, data and data record from recorded data of OSC, it gets the following table:

Table 2 Speed and frequency data

Sampling times	GPS speed（km/h）	DMI speed (km/h)	Rail speed (km/h)	Speed channel 1 Frequency (Hz)	Speed channel 2 TB5E-5 frequency (Hz)	phase difference of 2 channels
001	49	50	50	386.3	384.5	88.57
002				387.5	387.7	88.06
003				385.0	386.3	87.41
004				382.8	383.7	88.51
005				382.9	382.3	88.18
006	100	100	100	777.5	777.8	90.01
007				777.6	776.9	90.56
008				779.5	777.2	89.75
009				782.1	780.5	90.27
010				779.4	782.2	88.97
011	201	201	200	1567.3	1563.7	90.20
012				1570	1567	88.59
013				1568	1567	88.73
014				1569	1563	89.23
015				1571	1565	89.8
016	300	299	300	2328.5	2335.7	90.71
017				2335	2322	90.49
018				2334	2332	90.44
019				2324	2333	89.16
020				2335	2337	89.5

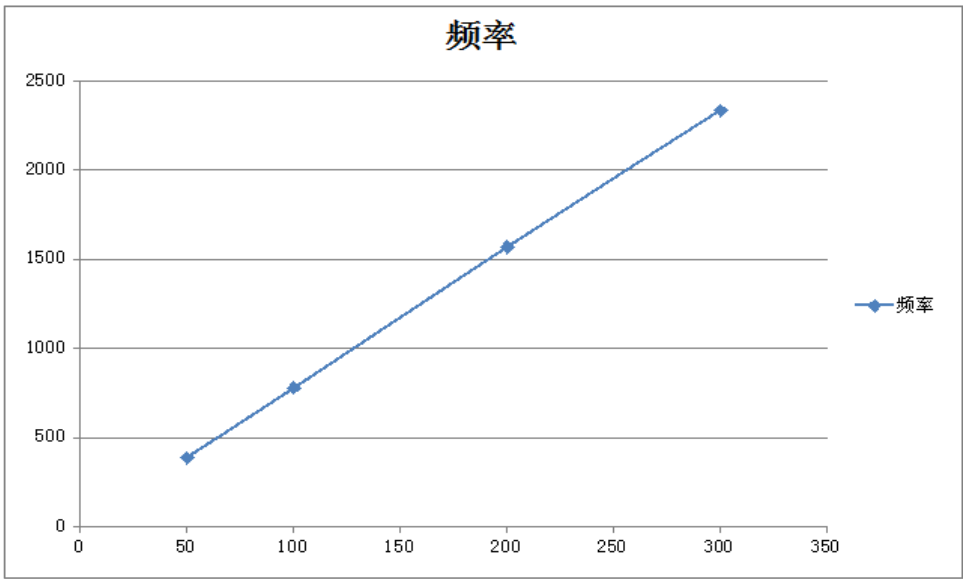

Diagram 6 Speed and frequency curve

Through analysis and calculation on test result, we can know that signal frequency and rail speed of speed sensor are linear relations, K_v=f/v=7.8. The signal generated by speed sensor is low value of 0V, peak value〉16.5V, the square signal with duty ratio of 0.5.

Analysis on performance and demand on simulated speed sensor

According to analysis on work principle of 2-phase speed senor, we can know simulated speed sensor should simulate the same speed signal with 2-phase speed sensor and transmit speed signal to SDU module, it is used to test whether performance of SDU module is normal or not. Therefore, this simulated speed sensor module needs to equip the following basic functions:

1）The generated signal should be the same with speed signal in wave form and phase generated by 2-phase speed sensor during rail running.

2）The frequency of generated signal can be controlled; it is used to simulate different rail speed.

3）Simulated speed sensor should be driven by SDU, when SDU inputs DC power of 18V, simulated speed sensor outputs speed signal.

4）The speed of high-speed rail is 0~350km/h, according to test result, signal frequency generated by speed sensor $f=K_v \cdot v$，simulated speed can generate square signal of 0~2730Hz.

Design plan of simulated speed sensor

According to analyzing the performance demand of the simulated speed sensor, we find we can use FPGA to realize the communication of simulated speed senor and the generation function of speed signal. FPGA can support serial communication, which meet demand of the communication between simulated speed sensor and upper computer. The DDS technology based on FPGA can realize generation of cycle wave form that can be controlled, meanwhile, FPGA supports hardware programming language and convenient for realization. By comprehensive consideration, we decide to use FPGA as core and prepare necessary peripheral circuit to realize the functions of simulated speed sensor.

Simulated speed sensor is divided into communication circuit, generation circuit of DDS square wave and peripheral amplification circuit. Of which, when simulated speed sensor is controlled by the upper computer, simulated speed communicates with upper computer by RS485 bus, which is used to receive command sent by upper computer and give corresponding feed back to upper monitor. The generation circuit of DDS square wave includes speed control module and generation module of square wave, the peripheral amplification circuit is driven by 18 V supplied by SDU, amplifies and outputs the square wave from the generation circuit. The function and structure

diagram is indicated by diagram 5.

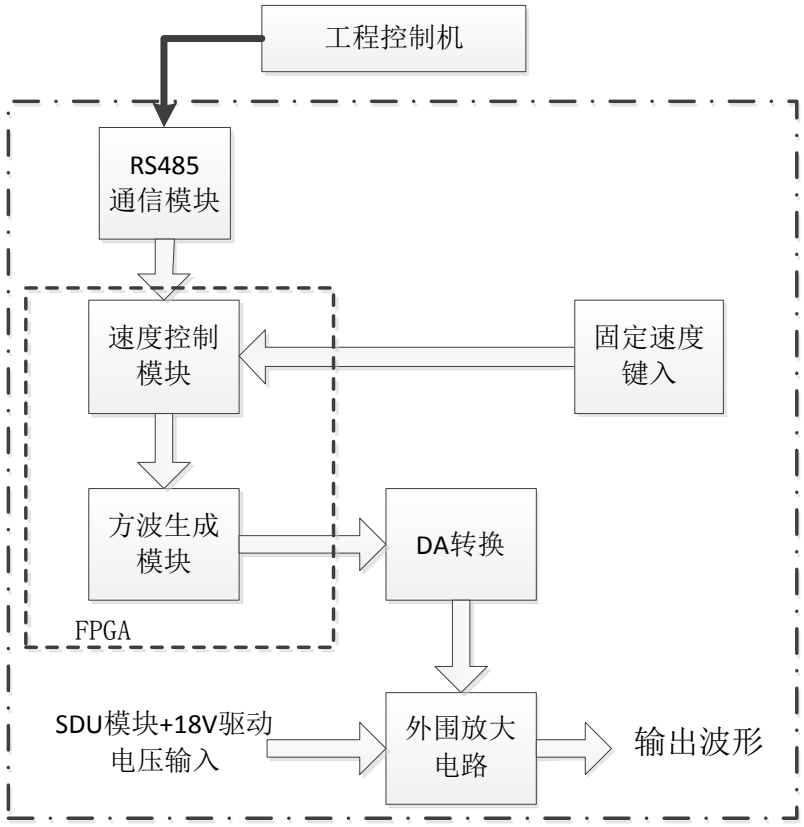

Diagram 7 Function frame

Principle and realization of communication circuit.

We use the full-separation ADM2587 chip from ADM company as the core of communication circuit. ADM2587E is a complete integrated and data-separation transceiver with protection function of ±15 kV ESD. It is applicable to high-speed communication applications. There is a integrated driver of RS-485 inside of the ADM2587 chip, which has one effective enable circuit drove by high level. It also provides one effective forbidden circuit of high level receiver, and it can make receiver output into high-resistance state. This part has characteristics of current-limiting and over-heat shutdown, which can prevent output short circuit as well as larger energy consumption caused by bus contention. The principle chart of circuit is indicated by the following diagram.

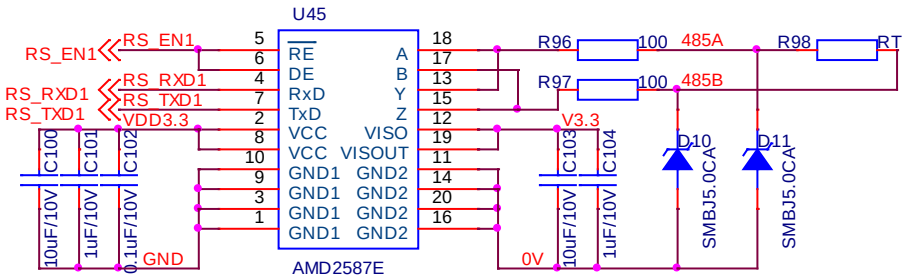

Diagram 8 Circuit principle chart of complete-separation RS485 interface

1)Communication protocol

Communication speed ratio between upper computer and simulated speed sensor is 9600 pbs, the form of data transmission is 8 data bits and 1 stop bit.

The data form sent by upper computer to simulated speed sensor:

Table 3 Data form sent by upper computer to simulated speed sensor

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Address	condition code	command1	command2	Data 1	Check sum

Table 4 The data content sent by upper computer to simulated speed sensor

No	Content	Byte	Content description
1	address	1	Address of simulated speed sensor is defined as CCH
2	Condition code	1	High 4 is 3 means that simulated speed sensor needs to reply on receiving information; C means that simulated speed sensor needs no reply on receiving information, low 4 is temporarily defined as 0.
3	Command 1	1	Command of acceleration or speed deceleration is defined as follows in details: 01H＝1 gear acceleration 03H＝2 gear acceleration 07H＝3 gear acceleration 10H＝1 gear deceleration 30H＝2 gear deceleration 70H＝3 gear deceleration AAH＝keep speed
4	Command 2	1	Set command of fixed speed and set as 68H
5	Data	1	The set fixed speed value, indicated by binary system, the maximum value is 255
6	Check sum	1	

Data form transmitted by simulated speed sensor to upper computer:

Table 5 Data form sent by simulated speed sensor to upper monitor

Byte 1	Byte 2	Byte 5	Byte 6
Address	answer-back code	Data 1	Check sum

Table 6 Detailed data content sent by simulated speed sensor to upper computer

No	content	byte	Content description
1	address	1	Address of upper monitor is set as 38H
2	answer-back code	1	Make reply by requirement of upper monitor, set as 11H
3	Data	1	Speed of simulated speed sensor at present
4	Check sum	1	

Realization principle of generation circuit of DDS.

DDS is the short term of Direct Digital Synthesizer in English, compared with the traditional frequency synthesizer; DDS has advantages such as low cost, low consumption, high resolution and quick conversion time etc. DDS technology is mainly composed of register for frequency control, accumulator of high-speed phase and ROM, of which, ROM needs storing the amplitude value of

the wave, which is transform into discrete signal，frequency control register can set frequency control code，which is used to control the generate frequency of generated wave form, while phase accumulator can traverse ROM at different speed cycle according to frequency control code, making amplitude value of the wave ,which is stored in ROM, output periodic, so that it generates periodic wave form. DDS chip generally outputs digital wave form, so it needs to pass high-speed DA converter to get one usable analog frequency signal.

DDS square generation circuit of simulated speed sensor is realized by FPGA programming, this design adopts chip of Cyclone IV EP4CE6E22C8 by Altera company, this chip adopts core of 1.2 V and 6272 logic units, 276480 RAM units and 92 IO channels, which can meet demand of DDS square wave generation on logic unit and multiple interface.

Generation circuit of DDS square wave includes speed control module and square wave generation module, the former generates frequency code and transmits to square generation module, the latter generates square wave with corresponding frequency by frequency code. When simulated speed sensor communicates with upper monitor, RS485 communication circuit transmits the received command from upper computer to speed control module; it generates corresponding frequency code by command. When it can't connect to upper monitor on site test, simulated speed sensor has a keyboard, which could inputs 3 fixed speed: 40km/h, 100km/h and 200km/h. Speed control module generates corresponding frequency code by input command.

Realization principle of signal amplification circuit.

Signal amplification circuit is responsible for procession and amplification on square wave signal generated by DDS square wave, the signal after procession is square wave signal with high level of 18V, low level of 0.5V. The operation amplifier adopts LF412ACH operation amplifier of LINEAR Technology, it is driven by DC power of +24V and -12V. +24V DC power is controlled by PS2501 opto-coupler. When the DC power of +18V supplied by the SDU shut down, the outputs end of opto-coupler is ended, the operation amplifier does not work, and the signal amplification circuit will not output square wave signal. When SDU inputs DC power of +18V, the output end of opto-coupler is gate on, +24 V power is supplied to operation amplifier, and the signal amplification circuit will operate and output square wave signal. In this way, we meet the demand that simulated speed sensor should be driven by SDU. When SDU outputs DC power of +18V, simulated speed sensor outputs speed signal. This amplification circuit almost has a splendid amplitude-frequency characteristic performance and a excellent phase-frequency characteristic performance within range of 0~20KHz, which can meet requirement of simulated speed sensor on signal amplitude and phase.

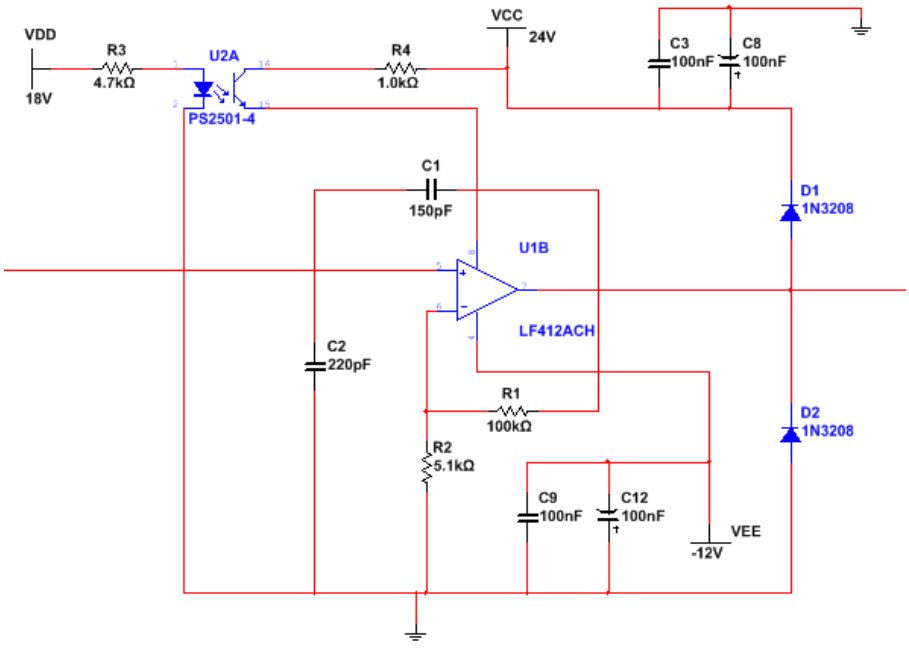

Diagram 9 Signal amplification circuit

Conclusion

According to the systematic study, we get the detailed work data of the speed sensor, which is used by high-speed rail. On this basis, we discuss the design plan of the simulated speed sensor based on DDS technology in details.

References

[1] Wang Hainan, Zeng Sheng, Wang Xixuan. In / miniature motor rotor special semi automatic dynamic balance correction system construction and research [J]. Chemical machinery, 2005, (01): 9-13.doi:10.3969/j.issn.0254-6094.2005.01.003.

[2] Kang Chengliang and lihuimin. Zhao Liangliang. For medium and smallsized motor rotors of automatic balancing machine design and implementation [J]. Modular machine tool & automatic processing technology. 2007, (02): 67-70.doi:10.3969/j.issn.1001-2265.2007.02.020.

[3] Xia Junchao, Zhao Liangliang, Zeng. The extraction and processing of the unbalanced signal of the rotor of small motor [J]. chemical machinery, 2007, (01): 8-11.doi:10.3969/j.issn.0254-6094.2007.01.003.

[4] Kang Chengliang and lihuimin. Zhao Liangliang. For influence coefficient of electric tool rotor automatic balancing machine calibration method [J]. Combination machine tools and automatic processing technology, 2007, (06): 23-26.doi:10.3969/j.issn.1001-2265.2007.06.007.

[5] Li Huimin, Zhao Liangliang, Zeng Sheng. Speed control and automatic positioning technology for automatic balancing machine [J]. motor and control application, 2007, (07): 24-27.doi:10.3969/j.issn.1673-6540.2007.07.008.

[6] Kang Chengliang, Zeng Sheng, Zhao Liangliang. Automatic balancing machine control system of multi machine communication in design and implementation [J]. Modular machine tool & automatic processing technology. 2008, (03): 53-56.doi:10.3969/j.issn.1001-2265.2008.04.015.

[7] Wu Jianping. Sensor principle and application [M]. Beijing: Machinery Industry Press, 2009

[8] Li, Yu Mei. Differential magnetoelectric relative vibration speed sensor development [J]. Sensor technology, 2003, (01): 25-27.doi:10.3969/j.issn.1000-9787.2003.01.008.

[9]ZHEN Y N, an d s, Chen B S. a speed calculation method for induction motor based on voltage decoupling control Principle.Power conversion Conference[M].Nagaoka: IEEJ/IEEE, 1997.573-578.

[10] Chen Shuo, SHUO M. based on flux observer of induction motor without speed sensor vector control system [J]. Transactions of China Electrotechnical Society, 2001, (04)

[11] Zheng Ping, Wang Mingyu. Speed estimation for sensorless vector control of induction motor [J].. Journal of, 2001, (05): 24-29.doi:10.3321/j.issn:1000-6753.2001.05.006.

[12] Zhu Wei, Chen Boshi. Based on the series dual model observer of induction motor without speed sensor vector control system [J]. Electric drive. 1997.9-11.

[13]A S MACY, R B Pandya, Xu Yong, Jing Tao. Neural network pattern recognition and its realization [M]. Beijing: Electronic Industry Press, 1999