Development of VLF Test System for Power Cables

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***Abstract*—with the rapid growth of the using of power cables in distribution network, a large demand for mobile high-voltage cable test systems is expected in the near future. VLF test system has a great equivalence of AC test, so it is wildly used in power cable test. In this paper, a novel VLF high voltage generator, based on LCC resonant converter, is introduced detailed. The Extended Describing Function (EDF) is used to select parameter of LCC resonant converter. In order to generate a true sinusoidal test voltage, the control strategy, concluding changing duty cycles of LCC resonant converter and load resistors, is proposed. The generator can generate a sinusoidal test voltage of 20 kV at 0.1 Hz and the result shows that the total harmonic distortion can meet the requirement of IEEE 400.2 standard.**

Keywords-VLF test system; power cables; extended describing function (EDF)

I. INTRODUCTION

As the bridge of power transmission, cable is an important part of power system. There are certain amounts of water in cable when it is manufactured, installed and used, which will contribute to water trees in cable. Water trees won't produce partial discharge, so it is difficult to discover. AC test has a good test result, but it is not easy to use in on-site test. Because with the increasing of length of the test cable, the devices of AC test become larger and heavier. Very low frequency (VLF) test system developed rapidly in recent years, which has a very good equivalence of AC test [1]. Not only withstand voltage test but also measuring of the dielectric loss Angle and partial discharge of the cable can be carried out by using VLF test system, so that comprehensive analysis on the status of the cable can be made easily.

In this paper, a novel topology of VLF high voltage generator is proposed. This generator is supplied by 220V, 50Hz Alternating Current. Firstly, alternating current becomes direct current after a rectifier. And then, the high frequency resonance current is produced in resonant cavity. Meanwhile, there is a high voltage on the power cables, which can be adjusted via changing the load resistance and the duty cycle of inverter. LCC series-parallel resonant converter, combining the advantages of series resonant converter (SRC) and parallel resonant converter (PRC) can reduce the EMI noise and switching loss.

II. BASIC PRINCIPLE OF TEST SYSTEM

The test system consists of two subsystems responsible for the positive and negative half waves. Except for the direction of high voltage silicon stack, the two subsystems are all the same, so that only one subsystem is analyzed in this paper. As illustrated in Figure 1, there are Rectifier Bridge, LCC resonant converters, high-frequency transformers, double voltage circuit and adjustable load resistor in a subsystem. In order to simplify the analysis, all the components in this circuit are considered as ideal components.

Once the topology of the circuit is known, a mathematical formulation for its behavior can be done. Based on the circuit illustrated in Figure 1, three nonlinear states can be obtained:

$$\begin{aligned}
\frac{di_L(t)}{dt} &= \frac{u_{AB}(t) - R_s * i_L(t) - u_s(t) - u_p(t)}{L_s} \\
\frac{du_s(t)}{dt} &= \frac{1}{C_s} * i_L(t) \\
\frac{du_{out}(t)}{dt} &= \frac{1}{C_o} * (i_D(t) - \frac{u_{out}(t)}{R_{out}})
\end{aligned} \tag{1}$$

The equation 1 cannot be solved because the number of unknown variables is much more than the number of equations. Through analyzing the circuit, Extended Describing Function (EDF) can be used for solving this task [2]. The variables in equation (1) can be approximated by its first-order coefficients or its zero-order coefficients of their respective Fourier series. So, they can be written as follows:

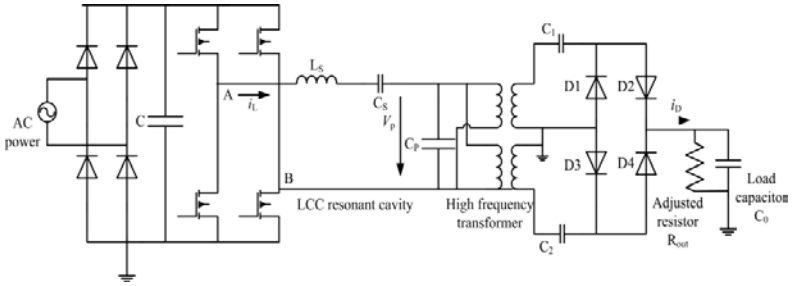

FIGURE I. POWER CIRCUIT OF THE SUBSYSTEM.

$$
\begin{aligned}
&i_L(t) \approx i_{LS}(t)*\sin(\omega t)+i_{LC}(t)*\cos(\omega t)\\
&u_s(t) \approx u_{SS}(t)*\sin(\omega t)+u_{SC}(t)*\cos(\omega t)\\
&u_p(t) \approx u_{PS}(t)*\sin(\omega t)+u_{PC}(t)*\cos(\omega t)\\
&u_{AB}(t) \approx \frac{\pi}{4}u_d*\sin(\frac{d*\pi}{2})*\sin(\omega t)\\
&u_{out}(t) \approx u_{oavg}\\
&i_D(t) \approx i_D(i_L, u_{oavg})
\end{aligned}
\tag{2}
$$

Through complex mathematical analysis [5], the equation (1) can be rewritten as equation (3):

$$
\begin{aligned}
\frac{di_{LS}(t)}{dt} &= \frac{1}{L_s}[\frac{\pi}{4}u_d*\sin(\frac{d*\pi}{2})*\sin(\omega t)\\
&\quad -R_S*i_{LS}-u_{SS}-\frac{i_{LS}*\sin^2\psi+i_{LC}*\mu}{\pi*Cp*\omega}+L_S*\omega*i_{LC}]\\
\frac{di_{LC}(t)}{dt} &= \frac{1}{L_s}[-R_s*i_{LC}-u_{SC}-\\
&\quad \frac{i_{LC}*\sin^2\psi-i_{LS}*\mu}{\pi*Cp*\omega}+L_S*\omega*i_{LS}]\\
\frac{du_{SS}}{dt} &= \frac{1}{C_s}*i_{LS}+\omega*u_{SC}\\
\frac{du_{SC}}{dt} &= \frac{1}{C_s}*i_{LC}-\omega*u_{SS}\\
\frac{du_{out}(t)}{dt} &= \frac{1}{C_o}*(\frac{\sqrt{i^2_{LS}+i^2_{LC}}}{\pi}*[1+\cos(\psi)]-\frac{u_{out}(t)}{R_{out}})
\end{aligned}
\tag{3}
$$

III. System Implementation

A. Resonant Parameter Selection

From the equation (3), it can be seen that once the value of C_P, C_S, L_S, f_S and the turns ratio are determined, both the dynamic response and the steady state response of the circuit can be deduced. Based on the dynamic response and the steady state response of the circuit, the optimal parameter can be decided. The parameter α (equal to C_P/C_S) has a great influence to the circuit performance. From the Figure (2), the higher the α, the higher the voltage gain and the resonant current. The smaller the α, the smoother the carve of normalized voltage conversion. According to the paper [3], the optimum range of α is 0.5 to 0.8. So α=0.5 is chosen.

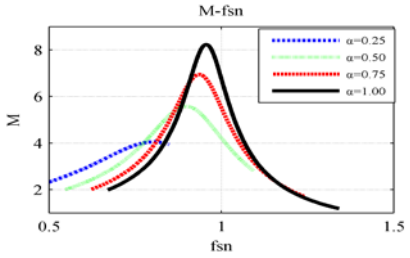

FIGURE II. CALCULATED NORMALIZED VOLTAGE CONVERSION VS. NORMALIZED FREQUENCY.

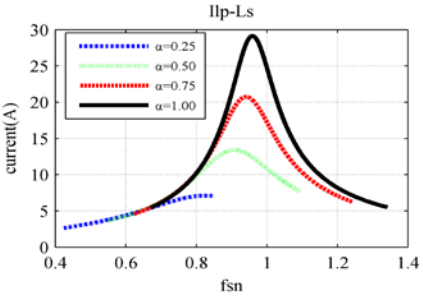

FIGURE III. RESONANT CURRENT VS. NORMALIZED FREQUENCY.

The peak of resonant current is an important parameter, which not only determines the maximum voltage of C_P、C_S and mosfet, but also reflects the power loss of the resonant circuit. Therefore, the peak of resonant current should be minimized. When the output voltage reaches the limit, the operation state is as follow: U_{in}=300V; f_S=25 kHz; n=30; I_L=5A; the series resonant frequency $f_0 = f_S / 1.2$; standardized coefficient of voltage and current are respectively 1.2 and 1.5[4]. The resonance inductor and capacitor can be calculated by the following formula.

$$
\begin{aligned}
&\frac{I_L}{I_{L\_N}} = \frac{U_{IN}}{U_{IN\_N}}*\sqrt{\frac{C_S}{L_S}} = \frac{5}{1.5}\\
&f_0 = \frac{1}{2\pi\sqrt{L_S C_S}} = 25000/1.2
\end{aligned}
\tag{4}
$$

After calculated, L_S=560μH;C_P=50nF;C_S=100nF. Taking the above parameters into the equation 3, the output voltage versus switching frequency f_S and duty cycle d are shown in Figure 3 and Figure 4. In order to expand the range of output voltage from 0 to 27kV, the best way is to adjust duty cycles.

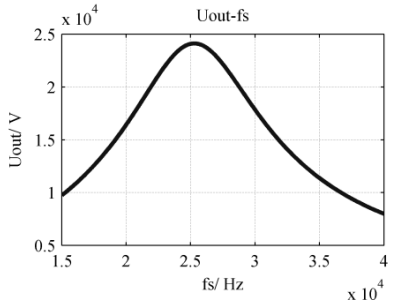

FIGURE IV. THE OUTPUT VOLTAGE VS. SWITCHING FREQUENCY.

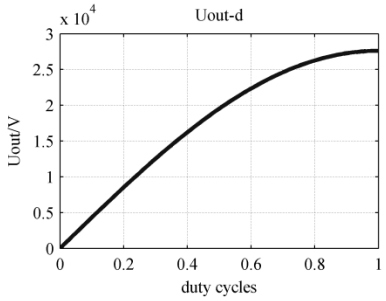

FIGURE V. THE OUTPUT VOLTAGE VS. DUTY CYCLES.

B. Control Strategy

From Figure 4, the output voltage will change from 0 to 27kV when duty cycles changes from 0 to 1, so we can regulate the output voltage by changing the duty cycles. Through analyzing the relationship between output voltage and duty cycles, output voltage is a linear function of sin (π/2*d) (Figure 5). Through the simulation, significant distortion can be found at zero-crossing point (Figure 6), so only changing duty cycles cannot get the true sine wave. This is because in the vicinity of the zero crossing point, the sinusoidal voltage has large variation rate, which is much larger than the voltage drop rate on load capacitance. Even though d=0, the output voltage doesn't drop rapidly. And then, significant distortion will happen.

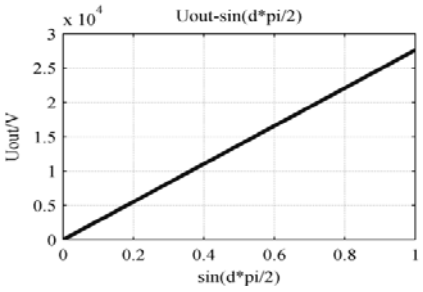

FIGURE VI. THE OUTPUT VOLTAGE VS. SIN(D*Π/2)/.

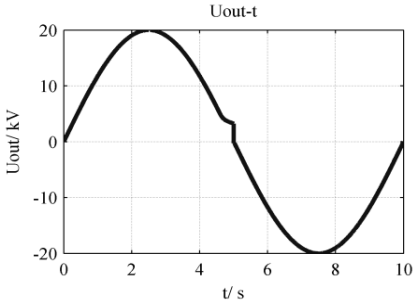

FIGURE VII. THE OUTPUT VOLTAGE WITHOUT CHANGE LOAD RESISTOR.

In order to improve the waveform, the large load resistor can be replaced by some small resistors in series, and each small resistor parallels with high voltage IGBT, shown as Figure 7. And then, sequentially close IGBT at the appropriate time to reducing output resistance and the time constant of the RC discharge. Coupled with the duty cycles change, the output voltage waveform distortion is small. Improved waveform is shown in Figure 8 and the block diagram of the control system is shown in Figure 9.

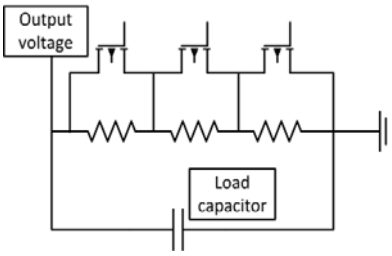

FIGURE VIII. IMPROVED LOAD RESISTOR.

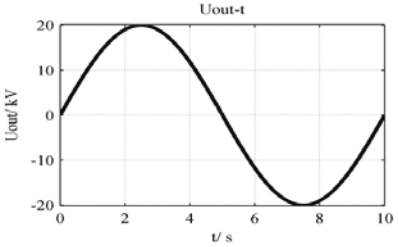

FIGURE IX. IMPROVED OUTPUT VOLTAGE.

At the beginning, duty cycle is 0, then the output voltage is 0 and the resonant current IL is approximately 0; when the output voltage doesn't equal to pre-set voltage which changes as sine, the Microprocessor calculate the △d and required output resistance. At the same time, the resonant current should be detected, if the resonant current exceeds warning value, duty cycles will be set as 0; if not, the program turns back to the next circulation.

The whole system is shown in Figure 10; the control system is implemented on a microcontroller which is integrated in the resonant circuit. The test cable is instead of a capacitor. Output voltage is shown in Figure 11, total harmonic distortion (THD) levels does not exceed 5%, so it can meet the requirement of IEEE 400.2 standard.

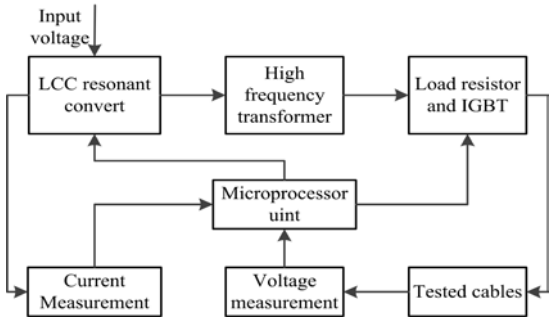

FIGURE X. THE BLOCK OF CONTROL UNITS.

IV. CONCLUSION

In this paper, a VLF high voltage test system based on LCC resonant converter is introduced. A design method of the LCC resonant converter is provided according to Extended Describing Function. The feedback control is used in this test system in order to achieve sinusoidal output voltage and

protect the circuit. Experimental results show the correctness and feasibility of the theory.

FIGURE XI. OVERVIEW OF THE TEST SYSTEM.

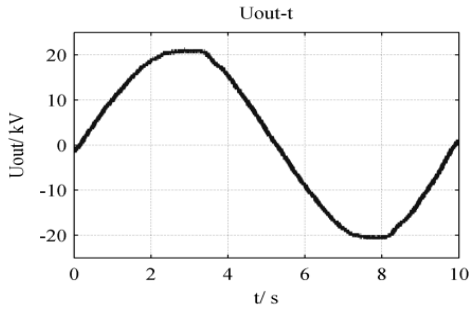

FIGURE XII. EXPERIMENTAL RESULTS.

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