Selection of Decoupling Capacitors for Power Delivery Networks with Multiple Power Ports

Q.D. Wang, Y.C. Wang, X.L. Li
State Key Laboratory of Power Transmission Equipment and System Security and New Technology
Chongqing University
Chongqing, 400044, China

Q.S. Liu
Chongqing Vehicle Test & Research Institute, National Coach Quality Supervision and Test Center
Chongqing EMC Engineering Technology Research Center
Chongqing, 401122, China

***Abstract*—in high-speed printed circuit board (PCB), decoupling capacitors are usually used to reduce noise of power ports. The number and location of capacitors is related to design cost and quality. This paper introduces a method to determine the suitable value and placement of decoupling capacitors for multiple power ports on the same board. Linear network theory is applied to characterize power delivery networks (PDN) with a high accuracy and then a PSO is customized for choosing decoupling capacitors, so that multiple-impedance of all power ports can meet the requirement of the target impedance after placing these capacitors. Finally, a practical board with specific capacitors was simulated and measured. The simulation and experimental results all meet the requirement of target impedance, which confirms the proposed method is valid.**

Keywords-decoupling capacitors; linear network theory; PSO; multiple-input impedance

I. INTRODUCTION

Generally, the connection of the chip to the power and ground planes (PGP) is represented by the power port. To maintain an acceptable power noise level, decoupling capacitors are put onto the PCB to decrease the impedance of power ports, while it will increase the power consumption and component costs. Therefore it is significant to select capacitors as effectively as possible. Some formulas derived from experience can help determine the suitable value of capacitor parameters [1]. Choosing capacitors including their types and locations can be automated by genetic algorithms [2-4].

Methods discussed above can help to lower PDN impedance successfully and they all focus on the PDN with only one power port. However, there are usually multiple power ports on the PCB. Power noise of these ports may interconnect with each other. In this paper, linear network theory is employed to characterize PDN as a group. Then this PDN is integrated with circuit models of capacitors to find the optimum values and locations of decoupling capacitors, which is processed by PSO technique.

II. IMPEDANCE OF POWER PORTS

When the voltage ripple tolerance for one power port is ripple, the target impedance is given by

$$Z_{target} = \frac{V_{dd} \times ripple}{0.5 I_{peak}} \tag{1}$$

Where V_{dd} is the supply voltage, I_{peak} is the maximum current drawn by the port over an entire clock period. Assuming that there exist n power ports totally, as shown in Figure 1, the target impedance of each power port can be calculated according to Eq. 1. In addition each port takes the input impedance as its PDN impedance. According to the linear network theory, the electric potential on port j is

$$\dot{U}_j = Z_{j1}\dot{I}_1 + Z_{j2}\dot{I}_2 + \cdots + Z_{jn}\dot{I}_n = \sum_{l=1}^{n} Z_{jl}\dot{I}_l \tag{2}$$

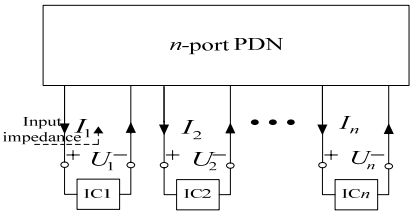


FIGURE I. DIAGRAM OF *N*-PORT PDN.

Hence, the input impedance of port j is then

$$Z_j = \frac{\dot{U}_j}{\dot{I}_j} = \frac{1}{\dot{I}_j}\sum_{l=1}^{n} Z_{jl}\dot{I}_l \tag{3}$$

Where Z_j is defined as multiple-input impedance of port j[5]. In the above calculation all effects of other power ports are reflected by the transfer impedance. Therefore the multiple-input impedance can characterize the power port with a high accuracy. On the contrary, if there is only one power port, self-impedance is often used as PDN impedance in traditional decoupling design.

III. SELECTION OF DECOUPLING CAPACITORS BASED ON PSO

A. Decoupling Design

In order to reveal the effect of a capacitor on the power port, the connection of a capacitor to the PGP is replaced by a new port, which is defined as capacitor port here. Firstly Z parameter of all ports can be extracted by numerical methods or measurement. When one capacitor is mounted or removed during iterations, Z matrix will be changed. Assuming that there exist p power ports and q capacitor ports in PDN, the power ports and capacitor ports are indexed as 1 to p and p+1 to p+q, respectively.

$$\begin{bmatrix} \dot{U}_1 & \cdots & \dot{U}_p \end{bmatrix}^T = \begin{bmatrix} \dot{U}_{p+1} & \cdots & \dot{U}_{p+q} \end{bmatrix}^T = \begin{bmatrix} \boldsymbol{U}_{ic} \mid \boldsymbol{U}_{cap} \end{bmatrix}$$
$$\begin{bmatrix} \dot{I}_1 & \cdots & \dot{I}_p \end{bmatrix}^T = \begin{bmatrix} \dot{I}_{p+1} & \cdots & \dot{I}_{p+q} \end{bmatrix}^T = \begin{bmatrix} \boldsymbol{I}_{ic} \mid \boldsymbol{I}_{cap} \end{bmatrix}$$
$$\left[\begin{array}{ccc|ccc} Z_{11} & \cdots & Z_{1p} & Z_{1(p+1)} & \cdots & Z_{1(p+q)} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{p1} & \cdots & Z_{pp} & Z_{p(p+1)} & \cdots & Z_{p(p+q)} \\ \hline Z_{(p+1)1} & \cdots & Z_{(p+1)p} & Z_{(p+1)(p+1)} & \cdots & Z_{(p+1)(p+q)} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{(p+q)1} & \cdots & Z_{(p+q)p} & Z_{(p+q)(p+1)} & \cdots & Z_{(p+q)(p+q)} \end{array}\right] = \left[\begin{array}{c|c} \boldsymbol{A} & \boldsymbol{B} \\ \hline \boldsymbol{C} & \boldsymbol{D} \end{array}\right] \tag{4}$$

$$\begin{bmatrix} \boldsymbol{U}_{ic} \\ \boldsymbol{U}_{cap} \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{B} \\ \boldsymbol{C} & \boldsymbol{D} \end{bmatrix} \begin{bmatrix} \boldsymbol{I}_{ic} \\ \boldsymbol{I}_{cap} \end{bmatrix} \tag{5}$$

Considering that capacitor port k(k=p+1,p+2,…,p+q) has capacitors in parallel in one capacitor port, as shown in Figure 3, current drawn by port k is

$$\dot{I}_k = -Y_k \dot{U}_k \tag{6}$$

Where Y_k is sum of the admittance of these capacitors. If there is no capacitor on port k, then Y_k is 0.

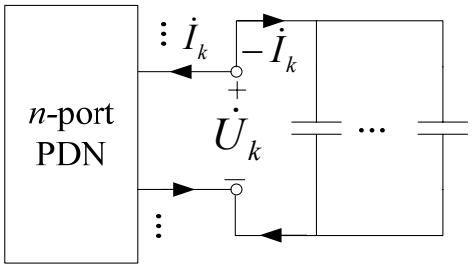


FIGURE II. DIAGRAM OF PORT WITH CAPACITOR IN PARALLEL.

Thus potential and current of these q ports can be written in a matrix form,

$$\begin{aligned} \boldsymbol{I}_{cap} &= \boldsymbol{Y}_C \boldsymbol{U}_{cap} \\ \boldsymbol{Y}_C &= -diag\left(Y_{p+1}, Y_{p+2}, \cdots, Y_{p+q}\right) \end{aligned} \tag{7}$$

When all capacitors and their ports are determined, Eq. 5 together with Eq. 7 can eliminate q capacitor ports. Then the Z matrix of p power ports after placing capacitor is derived by

$$\boldsymbol{Z} = \boldsymbol{A} + \boldsymbol{B}(\boldsymbol{I} - \boldsymbol{Y}_C \boldsymbol{D})^{-1} \boldsymbol{Y}_C \boldsymbol{C} \tag{8}$$

After that, the multiple-input impedance of the power ports is calculated by Eq. 3 and compared with their target impedance to determine whether decoupling design is acceptable or not. If not, PSO will change capacitors or their ports by iterations and YC will be changed at same time. After several iterations the Z matrix is optimized and finally the type of capacitors and their ports will be derived.

B. Optimal Technique

Particle Swarm Optimization (PSO) is inspired by the movement of birds while flocking. Each particle claims to be a solution of the problem within the search space, intending to attain optimal value of fitness, which is the objective function of optimization problem. In next iterations, particles keep the track of their best positions obtained so far and the best position among all the particles. Then their velocities and positions are updated by the following equations

$$\begin{aligned} v_i(t+\Delta t) &= \omega(t) v_i(t) + p_1 r_1 (x_l - x_i) + p_2 r_2 (x_g - x_i) \\ x_i(t+\Delta t) &= x_i(t) + v_i(t+\Delta t)\Delta t \\ \omega(t) &= (\omega_i - \omega_f)\frac{t_{max} - t}{t_{max}} + \omega_f \end{aligned} \tag{9}$$

Where x_i is the position of a particle and v_i is the velocity, t is the current iteration number, r_1 and r_2 are random numbers uniformly distributed in the range [0, 1]. The parameter ω is inertia who's initial and final values are respectively ω_i and ω_f, p_1 and p_2 are the acceleration coefficients. The x_g represents the best position attained by globally best particle and x_l is the best position gained by particle i so far. t_{max} is the maximum number of iterations. Since there are thousands of kinds of decoupling capacitors, PSO has advantage over some manual methods in searching the best composition of capacitors due to its global searching ability.

As mentioned in last section, some capacitor ports are set and marked in advance here. Then all capacitors are sorted according to their resonance points because the frequency range throughout which one capacitor has low impedance is associated with the resonance point. In this case study, the particle has two dimensions and can have discrete values only, one dimension represents capacitor number, and the other represents port number. When capacitor number and port number are initialized, they are corresponding with each other. Then fitness is determined by Eq. 10.

$$\min\ fit = N_C + \sum_{i=1}^{m} (\max(Z_i(f)) - Z_{it\arg et}) + P \tag{10}$$

$$P = \begin{cases} 0, \max(Z_i(f)) \le Z_{it\arg et} (i = 1,2,\cdots m) \\ k\sum_{i=1}^{m} \max(Z_i(f)), else \end{cases} \tag{11}$$

Where N_C is the number of capacitors chosen by PSO, $Z_i(f)$ is the magnitude of the multiple input impedance of power port i, $Z_{itarget}$ is the target impedance of power port i, m is the number of power ports, P is a penalty function and k is a constant such as 50. Eq. 10 and Eq. 11 are integrated into PSO to search the capacitor number and port number which contribute to the minimum value of fitness.

C. Practical Analysis

A practical board with two layers and a pair of PGP, was designed and manufactured, as shown in Figure.4. The board has 3 power ports (P1~P3) on the top layer and 16 capacitor ports (P4~P19) on the bottom layer. It also has a dielectric thickness of 0.4866 mm, and a metal thickness of 0.036 mm. The dielectric has a permittivity of 4.8 and a loss tangent of 0.02. There is one SMA connector attached to every power port. The SMA connectors are used to connect the port with the measuring instrument, Agilent E5061B Network Analyzer. The board including VRM, packages and bulk capacitors was modeled in Ansoft SIwave. The VRM is modeled by an inductor of 5nH in series with a resistor of 50 mΩ. There is a 10uF bulk capacitor mounted besides the VRM.

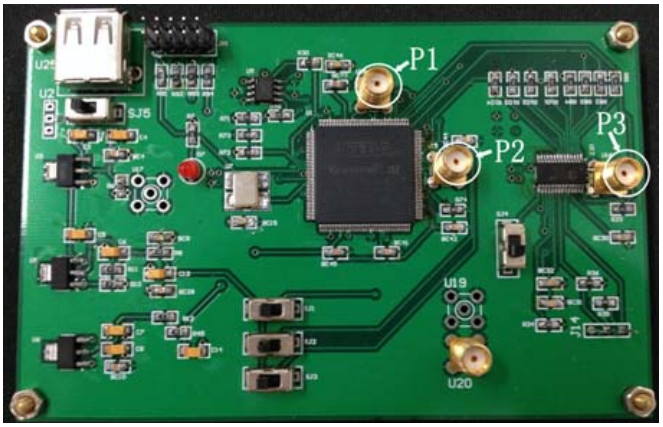
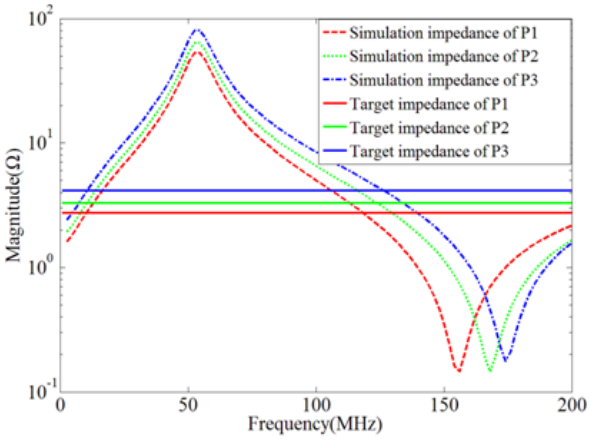
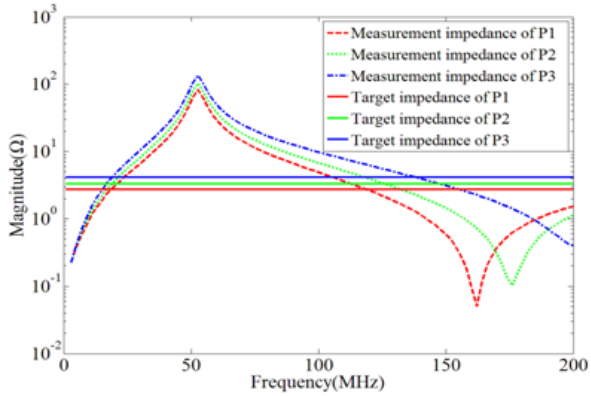


FIGURE III. A PRACTICAL BOARD FOR CASE STUDY.

The supply voltage of power ports is 3.3V. The maximum voltage ripple allowed is all 5% and maximum current is respectively 0.12A, 0.10A and 0.8A. According to Eq. 1, the target impedance is 2.750Ω, 3.300Ω and 4.125Ω, respectively. The frequency range of decoupling design is about 1MHz to 200MHz. When there are no decoupling capacitors on board, the calculated and experimental multiple-input impedance of the power ports is shown in Figure 5.



(a)



(b)

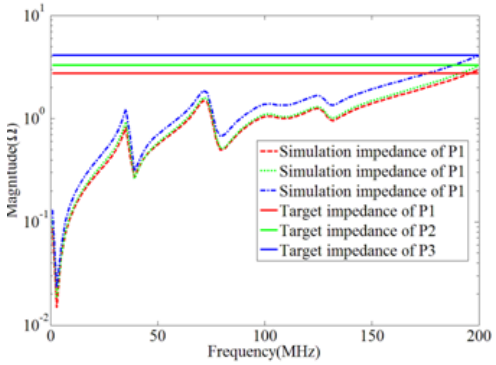
FIGURE IV. PDN IMPEDANCE WITHOUT CAPACITORS: (A) SIMULATION,(B) MEASUREMENT.

The simulation results agree with experimental tests. Traces in Figure 5 are not low enough in a very large frequency range, thus decoupling capacitors are picked out by PSO in this case and they are listed in Table 1.

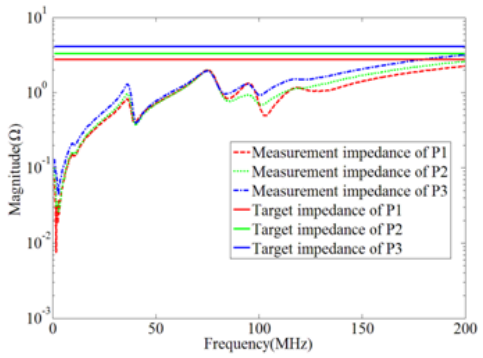
TABLE I. STYLES AND LOCATIONS OF CAPACITORS.

Capacitor Name	Manufacturers	Ports
CL21C471JBANNNE	Samsung	P5
CL21F103ZBANNNE	Samsung	P7
CL21C102JBANNNE	Samsung	P10
CL21F105ZAFNNNE	Samsung	P8 P9 P11 P14

Decoupling capacitors were mounted both in theoretical model and practical board. The magnitude of simulated and experimental impedance of the three ports after decoupling design is shown in Figure 6.



(a)



(b)

FIGURE V. PDN IMPEDANCE WITH CAPACITORS: (A) SIMULATION,(B) MEASUREMENT.

The behavior between simulated and experimental multiple-input impedance keeps the similar trend. The resonances of simulated results have little difference from those of experiment because the parasitic parameters caused by soldering capacitors in experiment may be not the same as those used in simulation and they are difficult to be controlled when frequency is high. In short, the results with selected capacitors by PSO are much better than those without capacitors and they meet the requirement of the target impedance.

IV. CONCLUSION

Linear network theory was used to describe the complex connection among multiple power ports of chips and it is proven that decoupling design based on multiple-input impedance has a high accuracy. Then optimal technique PSO was employed to select decoupling capacitors including their types, numbers and locations for multiple power ports at the same time. The selected capacitors are mounted on a practical board and consequently the decoupling results derived by experiments are acceptable.

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