8b/10b Encoder Design

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***Abstract*-In order to resolve the problem of base-line offset and unbalanced code flow during the fiber data transmission, thesis give a simple and practical solution:8B/10B encode. This solution taking an method which integrate checking scheme and logic operation, through Verilog HDL description language, realize the design of encoder. After lots of simulation and application, the results indicate: this amout of computation is small, quick speed, high reliability, and can achieve 8B/10B code function effectively.**

Keywords-8B/10B code, Verilog HDL language,Quartus Ⅱ9.0 software, Polarity deviation RD

I. INTRODUCTION

Due the quick development of communication of technology,fiber communication is more and more popular for people,at the same time,its higher transmission speed and bigger capacity are required by people. But, high-speed fiber transmission bring problem as base-line offset and unbalanced code flow. So, based on such problems, we design the 8B/10B encode, because its low transmission mistake percent and DC compensation function, also with checking mistake fuction during the transmission and special function[1], it resolve the problem as base-line offset and unbalanced code flow, but also was used in high-speed sbus.

On the way to complete 8B/10B. In local, it was designed to save the prepared code into an Programmable Read-Only Memory, this asimple method, but limit the speed of read. In foreign, it was finished by integrated logical circuit, that's mean to integrate total encoder into a small chip, was composed into a big special integrated encoder, its advantage is simple circuit, but the disadvantage is too complicated logic[2].

II. SOLUTION AND CONCEPT

In order to finish the encoder function during the fiber data transmission, we design the concept, which have three function model: checking mistake and special code、8B/10B encoder and FIFO. Disaplay in the Figure.1[3].

(1).Checking mistake and special code: For the input 8B, after checked mistake and special code, if have mistake or special code, it will output a symbol bit.

(2).8B/10B Encoder: transfer the input 8B into 10B as output, this function model is the core function of the concept.

(3).FIFO: FIFO data buffer.

III. ENCODER PRINCIPL

The principle of encoder is: mapping transfer the input 8 bits data into 10 bits data per the mapping principle, separate the 8 bits data into one group 3 bits data and another group 5bits data, after encoding of the 8B/10B encoder, output one group 4 bits data and another group 6 bits data, to make a 10 bite data, the situation of number 0 and number 1 together is three: 5 times number 0 and 5 times number 1; 4 times number 0 and 6 times number 1; 6 times number 0 and 4 times number 1. Above three situation have three unbalance 0,-2,+2 accordingly. During the process of encoding, mark this unbalance with an parameter :Polarity deviation RD . this polarity deviation RD is composed with RD- and RD+. RD- means the times of number 1 is 2 times more than the times of number 0 ; RD+ means the times of number 0 is 2 times more than the times of number 1 [4].

The original 8B data was separated into two part: front 3bits and back 5bits. For front 3bits, encoding it per 3B/4B; for the back 5bits, encoding it per 5B/6B. As show in Table.1. The order of original 8B data is HGFEDCBA, HGF encoded into fghj; EDCBA encoded into abcdei. So, the transferred 10B is abcdeifghj. After the transformation, the data flow was output by 10B . As show in Figure.2.

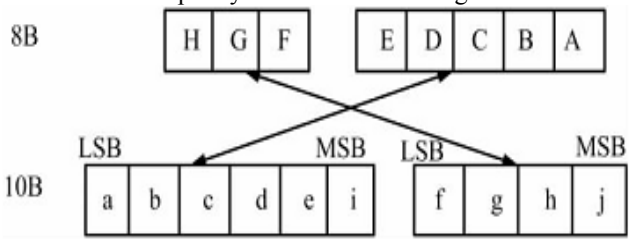

Figure 2. 8B/10B encoding relationship

It is important to ensure the DC balance of data flow during the transmission process, also need to think about the unbalance of DC data flow. As show in Table.2, for each 8B data, after encoding, it will be transferred into one kind of RD-&RD+. Encoder will decide the next 10B data based on previous RD and ensure the DC data flow balance .

The original status of encoder is RD-, it will check the data flow, if the quantity of number 1 and number 0 is the same, the polarity of next 10B data will keep RD-, otherwise, it will turn to be RD+. If previous 10B polarity is RD+, and the quantity of number 1 and number 0 of previous 10B data keep same, the polarity of next 10B data will keep RD+,

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otherwise, it will turn to be RD-[5].

IV. 8B/10B ENCODER DESIGN AND COMPLETE

The encoder design include three model: special code encoding, 3B/4B & 5B/6B encoding, RD control. This three model make the 8B/10B encoding characteristic, very clear and easy. As show in Figure.3.

Finished the process as below:

Firstly, you need to determine whether it is special character or not. If it is, there will be 12 kinds of code for special characters. Each character RD- and RD+ shall be matched with different 10B codes which is each inverted. According to the positive & negative of RD and output it with the homologous value of code. Otherwise run codes of 3B/4B and 5B/6B[6].

The code of 3B/4B and 5B/6B according to the mapping rule of the code of 8B/10B, through the look-up table method, use the Verilog HDL language to achieve it, find the 4B and 6B.

Let the 4B and 6B grouped to the 10B, and there are 4situations for this group: (1) when 4B and 6B are single value. (2) when 4B is single value and 6B is multiple-value. (3) when 4B is multiple-value and 6B is single value. (4) when 4B and 6B are all multiple-value[7].

Write the 8B/10Bencoder sequence by Verilog HDL language, the port of the encoder are made by 5 signals, there are clk, RSTn, kin, wr, dtin. Clk pin is the clock signal, RSTn pin is the reset signal, kin represent the dtin[7:0]special character input, wr is the enable signal[8].

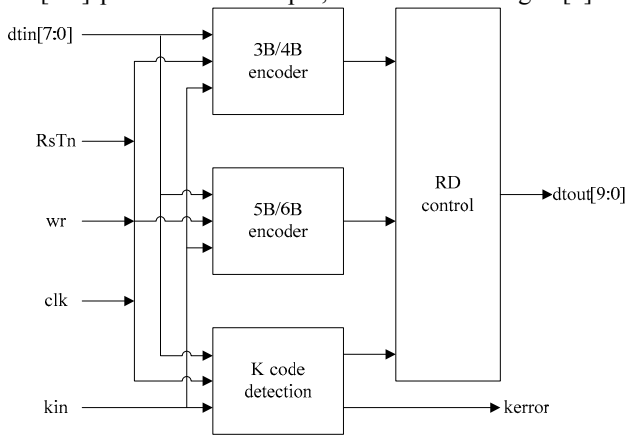

Figure 3. 8 B / 10 B code block diagram

V. EXPERIMENTAL VERIFICATION

In order to validate the effectiveness and feasibility of the above encoder design scheme. Based on high performance FPGA device, the simulation and integrated experiment is executed in the QuartusII9.0 integrated development. When kin is effective, the special characters streaming of illegal is input in dtin, the illegal mark signals Kerror will output effective high level which can be spotted in the simulation result, which illustrated the illegal code streaming was detected in the decoding circuit correctly. Decoding value 0101010101 was exported by dtout, simultaneously, which stated that decode can output by decoding circuit exactly, from the input and output of code streaming correspondence analysis, the problem of baseline migration and code streaming imbalance which appeared at optical fiber transmission data is solved by this plan very well. As shown in Figure.4. This program is suitable for integrated circuit and the FPGA design particularly, owing to its take less the FPGA internal resources，simple program structure, fast operation speed, low error code rate. Fully comply with the design requirements.

VI. CONCLUSION

The design of 8B/10B encoder is part of FPGA optical fiber communication, the demand of simple program logic relation, clear level demarcate, fast speed is put forward in the plan, which can be achieved by simulation. This program can be used in need 8B/10B encoder of optical fiber coding remote data transmission system.

ACKNOWLEDGMENT

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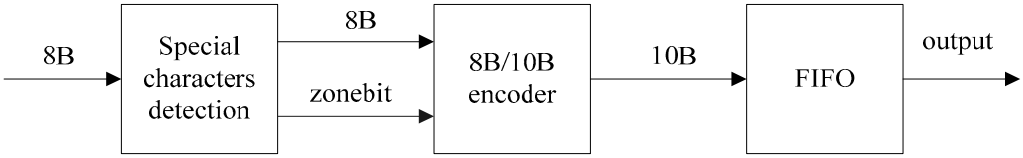

Figure 1. Function model

TABLE I. 3B/4B ENCODER

3B Decimal	0	1	2	3	4	5	6	7
3B binary(HGF)	000	001	010	011	100	101	110	111
4B binary（fghi）	0100/ 1011	1001	0101	0011/ 1100	0010/ 1101	1010	0110	0001/1110/ 1000/0111

TABLEII SPECIAL CODE ENCODING LIST

S.C. Byte Name	S . C. Code Name		HGF	EDCBA	abcdei	fghj	abcdei	fghj
K28.0	C0.0	(c00)	000	00000	001111	0100	110000	1011
K28.1	C1.0	(c01)	000	00001	001111	1001	110000	0110
K28.2	C2.0	(c02)	000	00010	001111	0101	110000	1010
K28.3	C3.0	(c03)	000	00011	001111	0011	110000	1100
K28.4	C4.0	(c04)	000	00100	001111	0010	110000	1101
K28.5	C5.0	(c05)	000	00101	001111	1010	110000	0101
K28.6	C6.0	(c06)	000	00110	001111	0110	110000	1001
K28.7	C7.0	(c07)	000	00111	001111	1000	110000	0111
K23.7	C8.0	(c08)	000	01000	111010	1000	000101	0111
K27.7	C9.0	(c09)	000	01001	110110	1000	001001	0111
K29.7	C10.0	(c0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(c0B)	000	01011	011110	1000	100001	0111

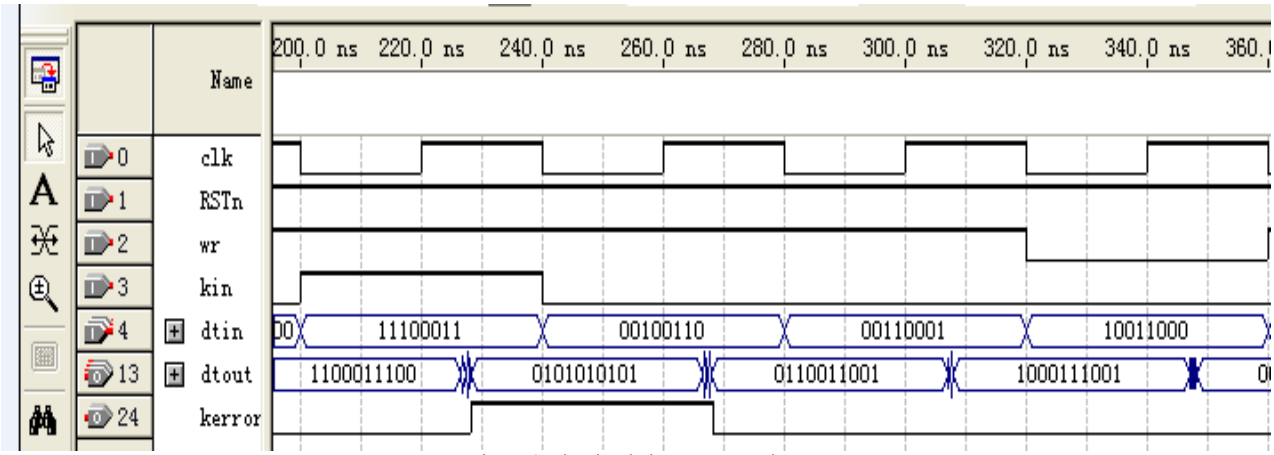

Figure 4. The simulation sequence chart