Design of IRIG-B Code Encoder Based on SOPC

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Abstract **-Aiming at the complexity of time unified hardware architecture, this paper presents the design scheme of IRIG-B encoder and system control based on SOPC. The NIOSII processor is configured with NIOSII IDE. Firstly, the design of IRIG-B(DC) coding module is accomplished to realize with Verilog HDL, and then IRIG-B(AC) coding module is completed successfully through the D\A conversion on the basis of IRIG-B(DC) code. The experiment result shows that the encoder can stably and reliably produce a standard IRIG-B code, and satisfy the application requirements.**

Keywords-IRIG-B code, SOPC, NIOSII, Time coding

I. INTRODUCTION

With the development of electronic technology, communications, deep space exploration, defense and other sophisticated technology applications present the strict requirements for the time synchronization[1]. In order to ensure the entire system in a unified and orderly work time scales, high-precision time system equipment is a key part of the system[2].

In the respect of the time synchronization equipment development, there is a large gap between China and the western countries. The extensive use of GPS receiver, large domestic quantities[3] are foreign company's OEM boards, such as Motorola, AshTech, Garmin, etc. The National Time Service Center's common-view receivers were purchased from abroad, which were used to receive the GPS signal, such as the TTR-6, 300T, R100 etc. The most high-precision time synchronization equipment-more than two-way satellite equipment was developed by the U.S. Atlantic[4]. At present, many domestic manufacturer also introduced time synchronization systems, the design was based on embedded microcontroller, which was the eight bit soft nuclear micro controller PICOBLAZE of Xilinx company[5] mostly, or circuit design, or accomplishing the IRIG-B coder with a single chip microcomputer, these designs can meet the practical engineering application basically, but the circuit was complexity, low accuracy, and the weak anti-interference ability[6]. This paper improves the IRIG-B coder based on SOPC, which uses large-scale programmable integrated circuits and a few interface circuit compatible peripherals[7]. Compared with the traditional design methods, the technology simplifies hardware circuit design, greatly reduces the cost, and improves system's reliability, flexibility and stability.

II. IRIG-B TIME CODE FORMAT PROFILE

IRIG code is standard time code[8], which was commander of the U.S. Committee. It is widely used in military, commercial, industrial and other areas. There are four parallel binary time code format and six serial binary time code format, and IRIG-B time code is the most common, which sends time information per second. The IRIG-B time code not only includes the information of second pulse, but also includes the information of the year, day, hour, minute, and second. Figure.1 is the IRIG-B (DC) code diagram. It is serial time code, the total width of each symbol is 10ms, a time-frame period includes 100 symbols, there are three kinds of coding of each symbol: binary "0", "1" and location identifier. There are three fields: the first is time field (years, days, hours, minutes, seconds), the second is control function field, the third field can respect the day time information by the use of binary symbol directly. Symbol's reference point is the pulse front, whose pulse width are 8ms, every 10 symbols have a location identification mark. Therefore, one second has a total of 10 location identifier: P1, P2, P3, ... , P9, P0, the pulse width of them is 8ms; PR is the reference point for the frame; binary "1" represents that the pulse width of symbol is 5ms, binary "0" represents that the pulse width of symbol is 2ms.

III. SYSTEM SCH VCEMATIC

As is shown in Figure.2, the system includes four main modules, Module 1: Obtaining the standard time; Module 2: Encoding; Module 3: D\A conversion; Module 4: IRIG-B(DC) code and IRIG-B(AC) code display. After getting the standard time through Module 1, Module 2 uses soft-core NIOSII[9]to compile the standard time into IRIG-B time code-second pulse, minute pulse, hour pulse, day pulse, and some control information, then the NIOSII sends the information to IRIG-B coding module which can compile it into IRIG-B(DC) code directly, Module 3 converses the IRIG-B(DC) code into IRIG-B(AC) code by the D\A conversion.

IV. IRIG-B CODING MODULE

After sending the standard time to the NIOSII module of encoder with the serial debugging assistant, then the NIOSII compile the standard time with C language programming according to the rules of IRIG-B code, generate IRIG-B pulse in the last. NIOSII encodes 100 bit BCD code pulse each sending one time, and send this 100 bit BCD code pulse to the encoding module, then the encoding module generates IRIG-B (DC) code.

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A. Configuring the NIOSII

Each SOPC system[10] should be analyzed the system's requirements firstly, and configure the basic hardware structure based on the task. Secondly, establish a QuartusII project. QuartusII project is a way to manage the design process. It stores the design file which is needed in creating FPGA configuration files. In this paper the project was entitled as des, then establish a des.dbf that is a top-level file format in this project. It likes printed circuit boards in designing circuit, soldering various function chips on the board. Then start the SOPC[11] Builder to create NIOSII system. Specific procedures are as follows:

1) Specify the target FPGA and clock settings;
2) Add NIOSII processor core;
3) Add system ID peripheral;
4) Add SDRAM Controller core;
5) Add a UART serial port module.

After configuring the soft-core, use NIOSII IDE software to develop applications. Then it can compile the system time into 100pps. Taking the second as an example, specific procedures are as follows:

1) Decomposing the second that was received by the NIOSII into a whole number plus a ten digit;
2) Converting each number from decimal to binary;
3) The index sign between The bit and ten flag, taking as "0" to process;
4) Output the binary number reversely in the second step ,plus the value of the index flag.

Minute pulse, hour pulse, and day pulse are similar to the second pulse, taking all the remaining bits as "0" to deal with. Second pulse, minute pulse, hour pulse, and day pulse according with the order, inserting index flag and the starting position, thus forms 100pps.

B. IRIG-B(DC) coding module

IRIG-B(DC) coding module was described with hardware description language Verilog HDL[12], Verilog HDL language is an excellent hardware description language, it is simple, efficient, easy to use, and powerful[12]. Because the IRIG-B code's frequency is 100HZ of square wave signal, and duty cycles are different. So the corresponding symbol was get by reasonable establishment with entering 1KHZ of square wave signal. Shuchu is a counter which was used to control the high width of the symbol, out1is a symbol counter which was used to control the width, when out1 reaches to 10, the symbol ct plus 1. When the ct is 100, 100pps coding is completed. Specific procedures are as follows:

1) Encoding module receives the value of Val from NIOSII.
2) When the value of Val is "0", output 2ms of high level, 8ms of low level. When the Val is "1", output 5ms of high level, 5ms of low level. When the Val is "Pr", output 8ms of high level, 2ms of low level.
3) Symbol counter ct plus one, and judge the symbol counter ct, if the value is 100, repeat step 1).

C. Experiment verification for IRIG-B(DC) coding module

Testing the hardware of encoder, after confirming that there is no questing, writing the program to the chip according to the design. In order to test easily, taking the computer system time as the standard time information, sent 00:00:37 to the FPGA through the serial debugging assistant. Theoretical waveform is shown in figure 3:

Observing the actual waveform shown in Figure.4 with the oscilloscope.

After the experiment, compared to experimental results and theoretical results, we can find that experiment results and theoretical results are consistent, because of outside interference, square wave signal has glitches.

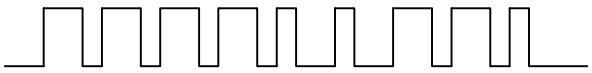

Figure.3 Theoretical waveform

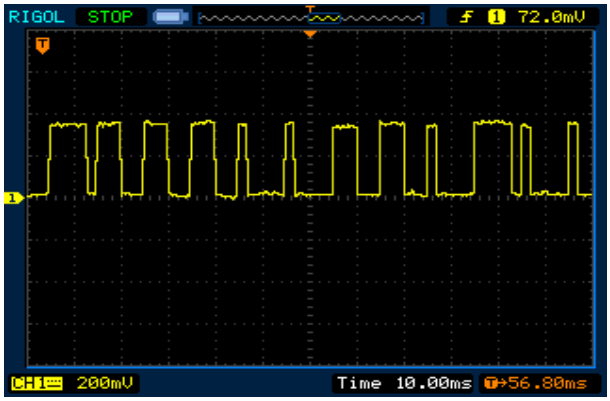

Figure.4 Actual waveform

D. IRIG-B(AC) coding module

1) sine wave signal generator module

According to DDS (Direct Digital Synthesizer) principle, it can produce a given digital waveform by the phase accumulated, in this design we use FPGA to accomplish N-bit phase accumulator and waveform memory. Phase accumulator can accumulate the binary code of frequency control word, the results could be make as the address for look-up table values of ROM, and this look-up table stores a cycle of sine wave amplitude[13]. Memory ROM output sine wave amplitude by in the reference clock-driven, if the phase accumulator is overflow, thus completing a cycle, its frequency is controlled by the frequency control word, the ROM's output drive the DAC, then it was converted into the analog sine wave.

2) sine wave modulation

IRIG-B code's frequency is 1KHZ, and it has been generated in 4.4.1. On this basis we only modulate amplitude. In the DAC circuit, we can select the DAC converter chip reference voltage through IRIG-B (DC) codes, when the IRIG-B is "1", DAC converter chip's reference voltage is high, when the IRIG-B is "0", DAC converter chip's reference voltage is low, the design is set

high-low ratio to be 5:3, so that we regulate the amplitude of the sine wave by the IRIG-B(DC) code , achieving the purpose of modulating amplitude.

E. Experiment verification for IRIG-B(AC) coding module

Sent computer system time to the FPGA through the serial debugging assistant, as is shown in Figure.5. Figure.5 is a section that is intercepted in the oscilloscope, and Figure.6 is a enlargement symbol. When the IRIG-B (DC) code is "1", IRIG-B (AC)'s amplitude is relatively high, when the IRIG-B (DC) code is "0", IRIG-B (AC) code's amplitude is relatively low, High-low ratio is 5:3, the encoder is stable, and reliable.

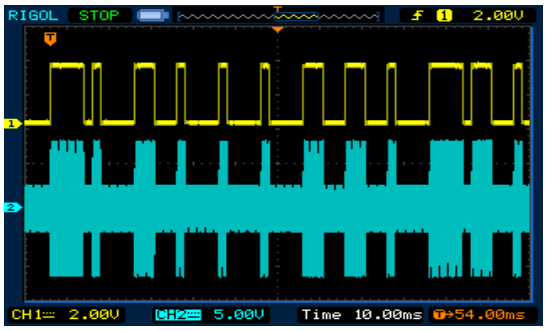

Figure.5 Actual waveform

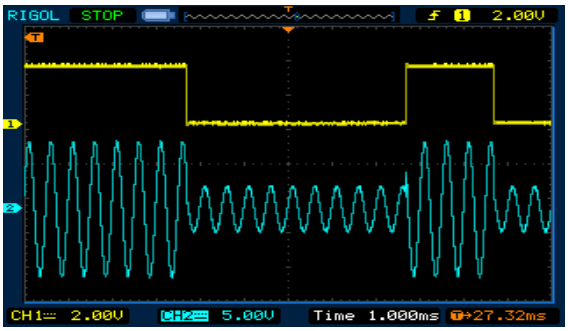

Figure. 6 Actual waveform of enlargement symbol

V. SUMMARIES

The Micro-processor based on FPGA which provides a simple instruction set can meet the needs of IRIG-B encoder. This paper makes NIOSII processor and the circuit of IRIG-B(DC) module into the FPGA device, so this design can save the storage space, I\O and other resources. Because of its flexibility and reusability of IP design for the complex system terminal design requirements, it can provide more efficient and more stable solutions. With the characteristics of flexible operation, convenient maintenance and system debugging, the encoder is easy to use. The experiment result shows that the design for IRIG-B coder based on SOPC is stable, punctuality, accurate, and reliable for data transmission, easy for operation and management, and it can achieve the design purpose.

ACKNOWLEDGMENT

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REFERENCES

[1] Qin Yi-li; Mu Dao-sheng. IRIG-B time code signal generator design. Ordnance Industry Automation[J], 2005 (6) , PP:80-81.
[2] Pang Ji-yao. FPGA-based IRIG-B encoder design. Modern electronic technology[J], 2009 (24) , PP:113-117.
[3] Fan Yi-qiang; Cao Jian. medium based on the B-code signal embedded technology in the sync pulse extraction method . Aviation Computing[J], 2005,35 (3), PP:25-27.
[4] Tong Gang; Cao Yong-gang; Chen Tao. MSP430+FPGA based on the IRIG-B time code system design. Electro-optical and Control[J], 2009,16 (5), PP:93-96.
[5] Hou Jian-hua; Wang Bao-lin. based on GPS satellite time and frequency synchronization principle study, military communication[J]s, 2010 (3) , PP:8-10.
[6] Liu Ming-bo, Geng-wen construction. IRIG-B code generation and demodulation system design and implementation. Research and development [J], 2010,29 (5) , PP:47-51.
[7] Shi Yu-qin. EPLD based on the IRIG-B encoder/decoder of the analysis and design. Modern electronic technology[J], 2007,30 (4) , PP:79-81.
[8] RIG Stand 200-98 IRIG Serial Time Code (Format B) [S].
[9] Ren Ai-feng, Chu Xiu-qin. FPGA-based embedded system design, Xi'an: Xidian University Press[M], 2004 , PP:70-85.
[10] Altera Corporation.Cylone II Device Handbook [Z] .2000.
[11] ZLG . SOPC-based embedded system tutorial. Beijing: Beijing Aerospace University Press[M], 2006 , PP:115-127.
[12] Wang Jin-ming Digital System Design and Verilog HDL. Beijing: Electronic Industry Press[M], 2008.10, PP:15-30.
[13] Wang Xiao-sheng; Sha Sheng-xian. based on the DDS Arbitrary Waveform Generator. Changchun Institute of Technology (Natural Science[J]), 2005,6 (2) , PP:56-5

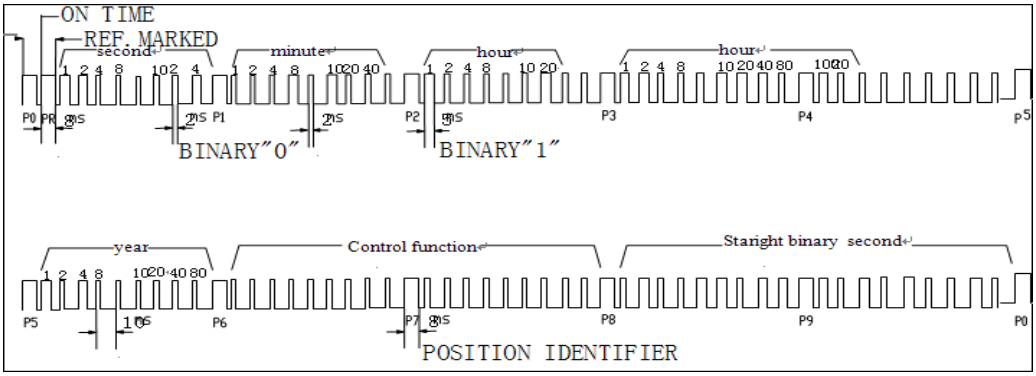

Figure.1 IRIG-B time format

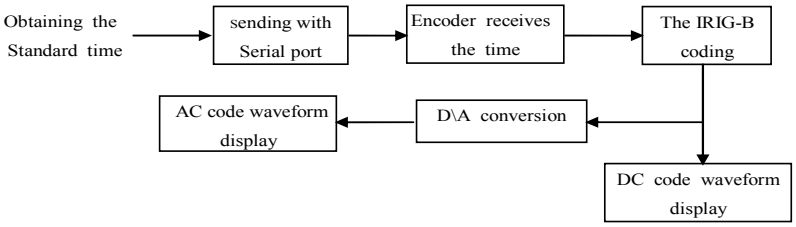

Figure.2 System schematic