A Novel Low Power CMOS VGA

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***Abstract* — A low-power Variable Gain Amplifier (VGA) is demonstrated in a commercial 0.18μm CMOS technology, with a chip size of 0.019mm^2. To compensate the threshold voltage process variation, a control voltage level shift (CVLS) methodology is proposed. The VGA was measured with a dynamic range of 29dB with a ±0.62dB error. The total power consumption is 186μW, and the bandwidth is 26MHz.**

Keywords—VGA; exponential current; low power; sub-threshold; linear-in-dB

I. INTRODUCTION

Variable gain amplifier (VGA), the gain of which is a linear-in-dB function of control voltage or current, plays an important role in stabilizing the power of the receiver's output. Current trends make the power-efficiency requirement become an inevitable consideration. However, one great challenge is the design of low-power VGA. Unfortunately, the power of traditional PNP, pseudo-exponential approximation, digital controlled amplifier and some other solutions for VGA are too big for portable receivers[1][2][3][4].

The sub-threshold methodology has been verified as a realistic low-power solution[5][6]. The well-proved exponential I-V curvature of MOS transistor is the base for sub-threshold circuit design [5][6][7][8].

$$I_{ds} = I_{s0} S \exp(\frac{V_{gs} - V_{th} - V_{off}}{nV_T})(1 - \exp\frac{-V_{ds}}{V_T}) \quad (1)$$

Where: S is the aspect ratio of the MOS transistor, V_{ds} is its drain and source voltage difference. V_T=kT/q (26mV@27℃). n is a parameter defined as the differential of the gate voltage V_G to the cut off voltage V_p, and it ranges from 1 to 2. V_{off} is the gate-source voltage tested when I_{ds}=0, which varies from different process, and for the current process, V_{off} =130mV. I_{so} is parameter defined by process.

When V_{ds}>4V_T, the last term of I_{ds} can be neglected, then the exponential I-V characteristic can be simplified as:

$$I_{exp} = I_{ds} = I_{s0} S \exp(\frac{V_{gs} - V_{th} - V_{off}}{nV_T}) \quad (2)$$

The above exponential I-V characteristic has been verified in low noise amplifier (LNA), voltage controlled oscillator (VCO) and voltage reference with satisfactory performance [5][6] [8].

As can be seen from Equation (2), I_{exp} shows a direct correlation with the threshold voltage V_{th}. However, as the threshold voltage may have great variation with the process. Thus, two main problems of the sub-threshold MOS transistor exsit: 1) MOS should be biased in sub-threshold region reliably; 2) the process variation of the threshold voltage V_{th} may drive MOS transistor out of sub-threshold region. Both these two problems can collapse the performance and even the function of the exponential I-V curvature.

The purpose of this paper was to present a low power VGA, where, the above two problems are compensated by a CVLS methodology.

II. CIRCUIT DESIGN

Fig.1 shows the configuration of the VGA. It is mainly composed of one stage of VGA amplifier cell (VGA-cell), which has two amplifiers in series, a V-I converter and a Vth-detector. The VGA-cell is the core circuit to realize the exponential voltage gain under the control of the exponential current I_{exp}, which is generated by the Sub-threshold transistor Mexp. To solve the problems of the sub-threshold transistor mentioned above, a CVLS scheme is introduced, which guarantees the Mexp always be biased in sub-threshold region and can simultaneously cancel the process variation. The summing resistor R0, V-I converter and the Vth-detector are the key circuits for CVLS, the theory of which will be demonstrated in the following text.

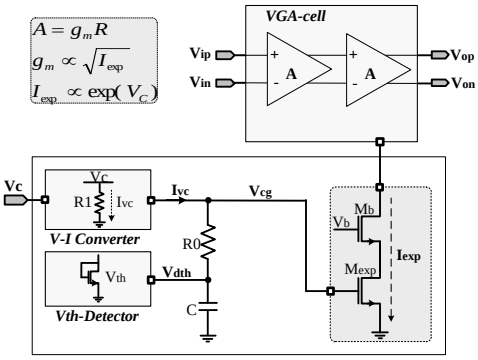

Fig.1. Architecture of the Proposed VGA

The schematic of the V-I converter is shown in Fig.2, and V_{cg} can be deduced as:

$$V_{cg} = V_{R0} + V_{dth} = \frac{MV_C}{NR_1} R_0 + V_{dth} \quad (3)$$

The schematic of the Vth-detector is shown in Fig.3. Transistor M3~M6 are biased in sub-threshold region with an exponential I-V curvature. The negative feedback loops formed by Amp1 forces V_{a1}=V_{a2}. Thus:

$$V_{\mathrm{dth}} = V_{\mathrm{th}} + V_{\mathrm{off}} + nV_{\mathrm{T}} \ln\left[\frac{nV_{\mathrm{T}}}{I_{s0}R_2S_3}\ln(\frac{S_5}{S_6}\frac{S_4}{S_3})\right] \quad (4)$$

When $V_{\mathrm{cg}}=V_{\mathrm{gs}}$ is applied on Mexp, I_{exp} can be then expressed as:

$$I_{\mathrm{exp}} = I_{s0}S_{M\,\mathrm{exp}} \exp\left\{\ln\left[\frac{nV_{\mathrm{T}}}{I_{s0}R_2S_3}\ln(\frac{S_5}{S_6}\frac{S_4}{S_3})\right] + \frac{MR_0}{NR_1nV_{\mathrm{T}}}V_C\right\} \quad (5)$$

The first item in the brace of the above exponential function and the coefficient of V_{c} can be considered as constants, which are supposed to be α and β respectively. Then:

$$I_{\mathrm{exp}} = I_{s0}S_{M\,\mathrm{exp}} \exp(\alpha + \beta V_C) \quad (6)$$

Which shows that I_{exp} is only decided by the control voltage V_{c}, as V_{th} variation is compensated by V_{dth}. Moreover, when all design parameters are reasonably set to make $(MV_{\mathrm{c}}R_1)/(NR_2)+nV_{\mathrm{T}}\alpha < |V_{\mathrm{off}}|$, $V_{\mathrm{cg}} < V_{\mathrm{th}}$ always holds. Thus, with the help of V_{dth} and CVLS scheme, transistor Mexp is always biased in sub-threshold region reliably even with large process variation. Similar deduction and simulation results related to above exponential I-V curvature have also been illustrated in the author's previous work[9].

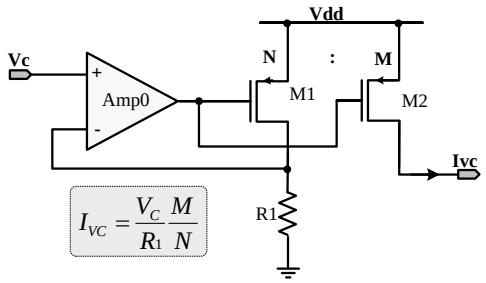

Fig.2. Circuit of V-I Converter

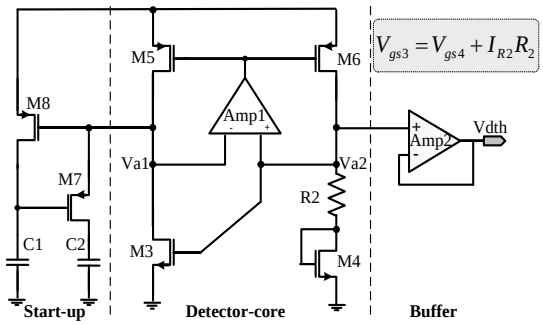

Fig.3. Schematic of Vdth-generator

The realization of the VGA-cell is shown in Fig.4, which is composed of two amplifiers in series. The trans-conductance of MOS transistor is: $g_{\mathrm{m}}=(u_{\mathrm{n}}c_{\mathrm{ox}}SI_{\mathrm{ds}})^{1/2}$. When control current I_{exp} is applied on the VGA-cell and based on Fig.1, the final gain of the VGA, G_{exp}, indicates an exponential gain of the VGA, which is shown as follows:

$$\ln(G_{\mathrm{exp}}) = \gamma + \alpha + \beta V_C \quad (7)$$

Where γ is a constant which can be expressed as:

$$\gamma = \ln(R_3R_4\mu_nC_{ox}S_{9\sim12}\frac{m}{2}I_{s0}S_{M\,\mathrm{exp}}) \quad (8)$$

Based on Equation (7), it should be noted that: as V_{th} variation of the exponential control current I_{exp} has been compensated by CVLS, the gain of the VGA-cell shows a linear correlation with the control voltage V_{c}. Finally, despite the great process variation of the MOS transistor, the proposed VGA has a good linearity.

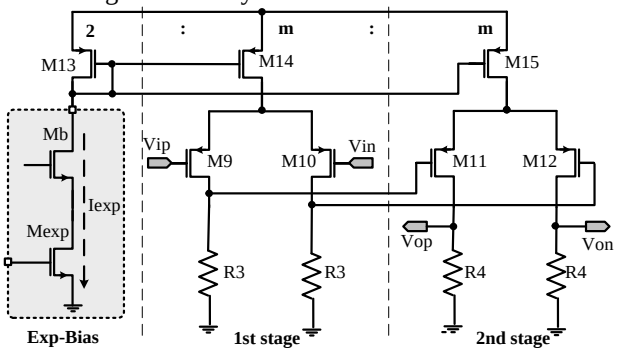

Fig.4. Schematic of VGA amplifier cell

III. MEASUREMENT RESULTS

The proposed VGA was fabricated in a 0.18μm CMOS technology. Fig.5 shows the die photo of the proposed VGA with a die area of 0.019mm^2.

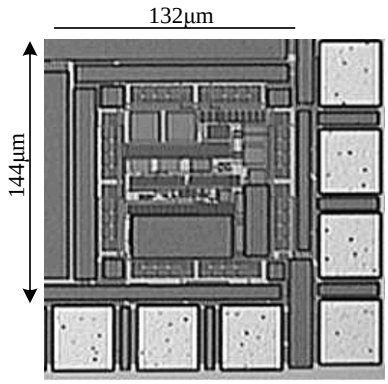

Fig.5. Die photo of the proposed circuits with test pads

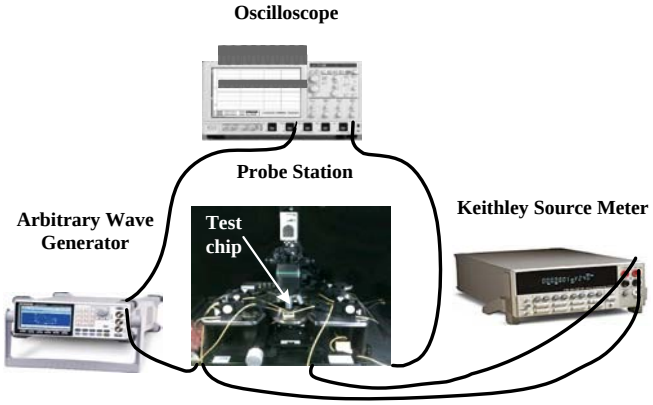

Fig.6. Diagram of the test setup

The performance measurements of the proposed VGA are made on-wafer with the help of a probe station. The diagram of the complete test setup is shown in Fig.6, where the

sinusoidal input is generated by an arbitrary wave generator. Moreover, a Keithley source meter is used as the power source of the VGA, which can simultaneously be used to detect the current consumption of the VGA.

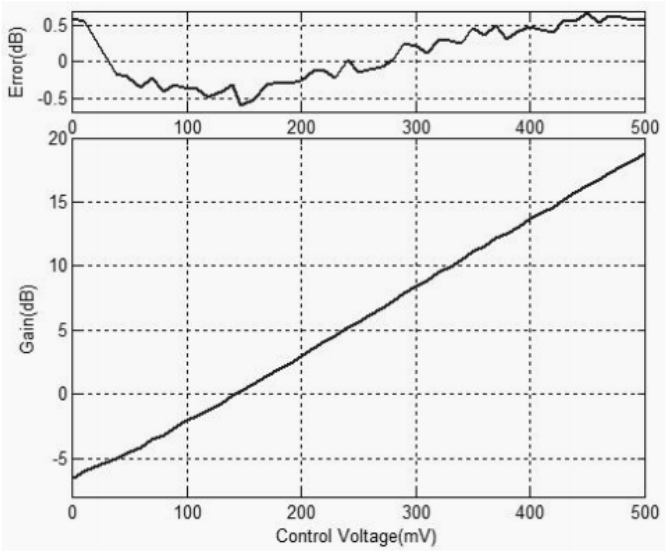

Fig.7. Gain and dB error with respect to V_c

The measured gain of the proposed VGA is shown in Fig.7. As can be seen, with the control voltage V_c ranging from 0 to 500mV, the dynamic decibel range is up to 29dB, and the dB-error is less than ±0.62 dB.

Table 1 shows the performance of the proposed VGA compared with previously reported VGAs. The total power consumption is 186μW, which is tested by the Keithley source meter.

TABLE I. Performance summary of the Proposed VGA

Parameters	This Work	[1]	[2]	[4]
Power source/V	1.8	1.8	1.8	1.8
Number of stages	1	1	3	3
Gain range/dB	29	48	60	95
dB error/dB	±0.62	NA	NA	NA
Bandwidth/MHz	26	3	16	32
Power/mW	0.186	0.55	3.6	6.5

IV. CONCLUSION

A low power VGA is demonstrated with a power of 186μW, where the CVLS scheme compensates the V_{th} variation and safely biases MOS in sub-threshold region. As a result, the VGA shows good linearity even under big process variation. The measured dynamic range is 29dB, and the dB-error is less than $\pm$0.62 dB. The bandwidth is 26MHz, which is big enough for Zero-IF receiver.

ACKNOWLEDGMENT

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REFERENCES

[1] Shang Hisen Yang, etc, A 48-dB dynamic gain range/stage linear-in-dB low power variable gain amplifier for direction conversion receivers, IEEE J. of Solid-State Circuits, vol. 38, November, 2011, pp. 1602–1608.

[2] Q. Q. Lei, etc, A Low-power CMOS VGA with 60-dB linearly controlled gain range for GPS application, 2008 IEEE Solid-State and Integrated-Circuit Technology, October 2008, pp. 1669-1675.

[3] D. G. Liang, Q. Ye, A 96-dB CMOS programmable gain amplifier for Low-IF receiver, 2008 IEEE Communication, Circuits and Systems, pp. 101-104, May 2008.

[4] Q.-h Duong, etc, A 95-dB linear low-power variable gain amplifier, IEEE Tans. Circuits Syst. I. vol. 53, pp. 1648-1657, Aug. 2006.

[5] Hanil Lee, etc, A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications, IEEE Microwave and Wireless Components Letters, Vol. 17, No. 11, Nov. 2007.

[6] H. Lee and S. Mohammadi, A 3 GHz subthreshold CMOS low noise amplifier, in Proc. IEEE RFIC Symp., Jun. 2006, pp. 494–497.

[7] Weidong Liu, etc, BSIM3v3.2.2 MOSFET Model Users' Manual, Department of Electrical Engineering and Computer Sciences University of California, Berkeley, CA 94720.

[8] Yongqian Du, et al., A reliable demodulator and a power regulation circuit with an accurate and small-size voltage reference in UHF RFID, Microelectron. J. 44 (2012), pp. 72-79.

[9] Du Yongqian, Zhuang Yiqi, Li Xiaoming, and Liu Weifeng, New Type of Low-Power Exponential Current Generator for VGA. Journal of University of Electronic Science and Technology of China. Vol.43, No.2, Mar. 2014, pp. 282-286.