# An Example of Network Video Monitoring System Based on DM6446

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**Abstract.** Design and implementation of a network video monitoring system, whose master chip is the DM6446 of TI DaVinci series which combines the digital signal processing technology, is introduced in this paper. The hardware of this system is with simple interface and the software is with perfect function. The testing results indicate that this network video monitoring system is designed with high stability, good image quality, good network transmission performance, and has good practical applications. The strong ability in data processing is shown.

## Introduction

With the development of network technology and in-depth information technology, video surveillance, security surveillance applications[1,2] and related industries began to enter the network age, so for the security industry, especially video applications, network monitoring and management functions and network adaptability have become increasingly demanding high. Monitoring network users demand increasingly prominent, not only to achieve local control, but also hope that through the remote, even through wireless monitor, which only the network to meet the needs of users. From the front-end video capture, video data transmission, to back-end video management, and even to video storage have a close relationship with the network. On the basis of DaVinci development board, this article effectively used of high-end 32-bit microprocessor (ARM + DSP) processing power, made a complete embedded network video surveillance system design, completed a design on video surveillance system based on DM6446.

## The DM6446 Processor

For TI, the demand for high-end video multimedia system design introduced DMSoC (Digital Media System on Chip) series dual-core processor, which uses TI's DM6446 DaVinci technology, the chip is 361 pin BGA package. It consists of chip system control module, ARM subsystem, DSP subsystem, VICP (Video Image Co-Processor), Resource Exchange Center (SCR), VPFE (Video Processing Front End), VPBE (Video Processing Back End), the external control Module, and external storage module. Structure is shown in Fig. 1.

DM6446 [3,4]has a wealth of resources and computing power, particularly for digital video applications, mainly characterized by the following: (1) High Performance; (2) A dedicated video processing subsystem; (3) Large storage capacity; (4) A large number of peripherals; (5) Low power, multiple power management modes.

## System Structure and Function Design

The system is based on TMS320DM6446 (abbreviated as DM6446) core processor, which consists of the video acquisition and processing module, video display module, ether-net transmission module, memory module, power module and control module and other peripheral parts. System structure and function block

 

diagram shown in Fig. 2. DM6446 video processing chip, dual-core architecture, combined with TI, TMS320C64Plus DSP processing core high-speed signal processing features and ARM926EJ-S RISC complex peripheral control, with complex and high-end peripherals (such as: high-speed video decoder[5,6], high-speed network transmission Transceivers, etc.), can fully satisfy the real-time video processing with large computational needs.

System circuit used the video capture module to capture video images, the DM6446 chip to control, stored the video images to hardware modules DDR2 SDRAM through the Data Exchange Center (SCR). The system then calls the video processing algorithms, network transmission, the local hard disk storage modules, complete video surveillance capabilities.

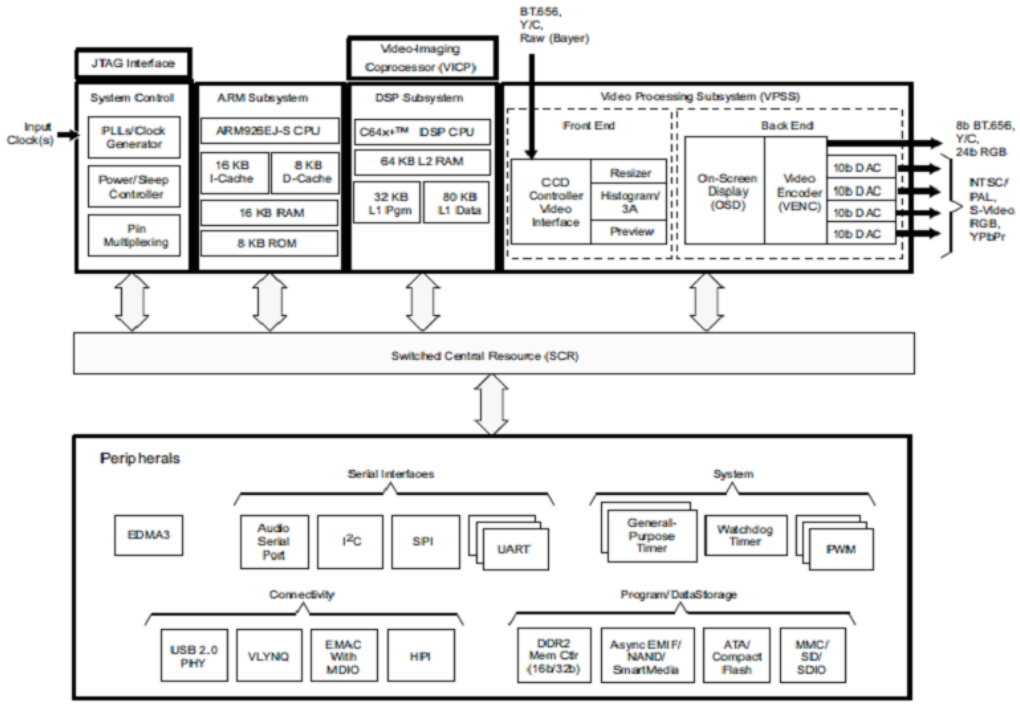


Fig. 1 Functional block diagram of DM6446

## Hardware Module Design

The following mainly describes the design analysis of the video decoder module and video display module.

**Video decoding module.** TMS320DM644+ series multimedia processors[7,8] have dedicated video ports, be seamless connectivity with video codec chip. Video port is designed specifically for digital video applications, high-speed parallel interface, as opposed to general-purpose DSP chips need to be added early FIFO chip access EMIF interface design structure, dedicated video port transfer rate greatly increased, a corresponding decrease development effort. Fig. 3-1 for the DM6446 block diagram of the video port.

Video interface includes a video processing front-end and back-end video processing. Video processing subsystem provides a video input interface (video processing front end), the interface can be connected to image sensors, video decoders and other video input signal; while the subsystem for analog standard definition television, digital LCD panels, HDTV encoder peripherals provides a video output interface (video processing back end).A common buffer and DMA controller are provided inside the chip to ensure efficient communications between DDR2 and video processing subsystem. Video processing front-end including the CCD controller (CCDC), the image preview engine (IPIPE), the hardware device 3A budget statistics (H3A), scalar, and histogram. In a word, these modules include a powerful and convenient front-end video interface.

**Video Display Module.** For real-time display of video captured by CCD images in this project, the application design of the video display thread to complete. While taking advantage of DM6446VPBE (video back-end) OSD (PIP) technology to synchronize the video display window shows the video capture frame rate, bit rate, acquisition time and other important parameters.

Through the main function call pthread_create function to create the main video display and set the video display thread main function entry address of the thread, the thread is successfully created, the system automatically jumps to that address video display thread started main function, the main function of the main function call pthread_create to create video Showing threads, the thread running argument (arg parameter) data structure is as follows:

```
typedef struct CtrlArg{
Rendezvous_Handle  hRendezvousInit:
Rendezvous_Handle  hRendezvousCleanup;
VideoEncoder       videoEncoder;
ehar               *videoFile;
int                time;
}CtrlArg;
```

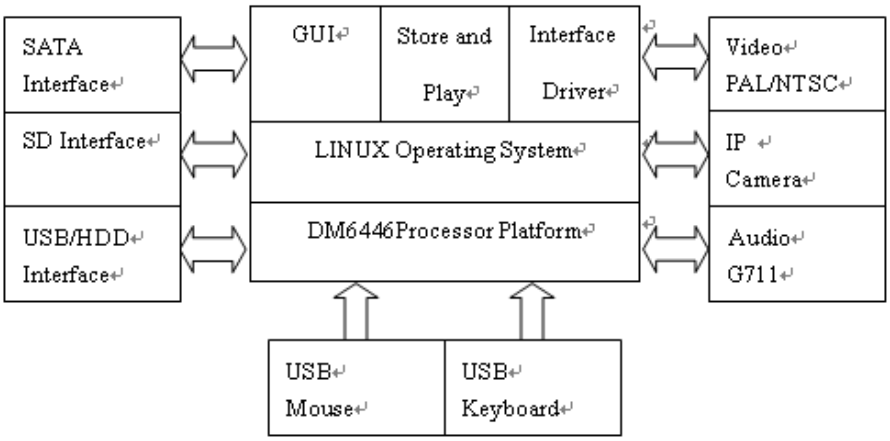


Fig. 2 System structure and function block diagram

## System Software Design

The software part of the video surveillance terminal [9,10] should include video capture, video playback, video compression and video data transmission and other basic tasks. TI, for this complex multi-tasking applications published DSP / BIOS package, DSP / BIOS is a simple real-time multitasking operating system, is a real-time processing cores that can be cut. It has many features real-time operating systems, such as task scheduling management, synchronization and communication between tasks, memory management, real-time clock management, interrupt management, driver management, and other peripherals. The system is based on TI's DSP / BIOS design software part of the design.

Five system tasks were defined, including image input task (function _tskVideoInput), image coding tasks (function _tskProcess), control tasks (function _taskControl), network tasks (function _network_main), the idle task (Function IDL_F_loop). Once the DSP / BIOS starts, DSP / BIOS will schedule between these types of Task. When there is no the first 4 tasks or hardware interrupt task, it will perform the task of calling the function for the IDL_F_loop idle loop process, implement the IDL background thread. Through a variety of messages between the various tasks to complete the synchronization and communication, video input frame will send a message fromInputtoProc to inform the video processing task (tskprocess) when it is ready. After

video compression is completed, the message fromProctoInput need to tell the mission and then capture the next video input Frames, also need to tell the network through messages fromProctoNet transfer tasks (Network) network transmission of video streams, and also need to inform the video output message fromProctoOut task (TskVideoOutput) local display video. Messages between the various missions are sent in both directions

Codec Engine is a software module between applications and the specific algorithm. The relationship between Codec Engine and DSP is similar to the relationship between the client and application server, the essence is the RPC realization on the dual-core. At this point, we can see ARM as a client-side, DSP as a server. In the ARM side, in terms of video-type applications, the application first collected the original image signal by VISA API calling related to Codec stub function is called by the stub functions that related to Engine API functions. However, the actual Codec algorithms run on DSP, so the signal must be carried out by the Codec Engine package, through the operating system abstraction layer to communicate with the DSP and then sent data package.

When the data was sent into DSP, DSP algorithms instances received related data information. This time, the received data is encapsulated before, it must be analyzed by DSP-side skeleton (Skeleton) ,and gain a call VISA interface parameters, and then call the relevant instance of DSP-side algorithm. The methods returning the data that processed by DSP-side algorithm to the application is opposite to the previous data incoming process.

## Summary

This article used the advanced Davinci technology, designed a DM6446 network based video surveillance system, the system program has high stability, good image quality, fast processing speed, and good network transmission performance. At the same time, it used the embedded hardware system design, the integration becomes higher. This design was proved to be a development program which had a good practical value.

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