

# The Real-time Acquisition Terminal System Based on Multi-machine Parallel

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**Abstract**—This paper describes a real-time acquisition terminal system based on multi-machine parallel, which utilizes multi-CPU interconnect technology based on SPI bus. Up to 10Mb / S speed full-duplex communication is used between the CPUs. Through exclusive signal lines so that the CPU can access external devices without conflict, Based SPI bus characteristics proposed two different parallel multi-machine communication strategy. It has obvious advantages in improving the system processing speed and reduce network latency, real-time and improve system reliability, etc.

**Keywords**-SPI; multi-machine; exclusive signal line; real-time; acquisition terminal system.

## I. INTRODUCTION

As market competition intensifies, the performance and cost have become increasingly demanding. Multi-machine real-time control systems have become highly intelligent industrial enterprises in the production control system of choice for high-tech. However, due to limitations of embedded systems with limited resources, multi-machine parallel real-time system become a serious problem. Multi-machine parallel system in the application process need to do a lot of monitoring data (video, images, audio, etc.) collection. Collecting data for a large number of processing often requires resource-intensive. Originally limited resources on embedded terminal system poses a great challenge. How in the case of limited computing resources to further improve system response speed to meet the growing demand for real-time research becomes a problem which need to be resolved. On the other hand, when the remote control terminal embedded by limited network bandwidth, how timely and reliable control commands is sent to the destination. This is a solved problem of the terminal system.

## II. FUNCTIONAL DESCRIPTION

### A. SPI principle introduced

SPI is an acronym of serial peripheral interface. SPI is a high-speed, full-duplex, synchronous communication bus. His pins on the chip occupies only four lines, which save the number of chip pins, so that can be saving space for the PCB layout convenience. SPI communication principle is very simple. It is a master-slave mode work. This pattern usually has a master device and one or more slave devices. SPI needs at least four lines, you can use only three lines in a one-way

transmission. These four lines are all based on the SPI devices in common, they are SDI (data input), SDO (data output), SCLK (system clock), CS (chip select). SCK provide clock pulses to communications. SDI and SDO are data transfer completed based on the SCLK. Data output through the SDO line, rising or falling edge of the clock data is changed, the falling or rising immediately be read to complete a data transmission. Data input can also use the same principle. Thus, at least eight times change (upper edge and a lower edge of one) of the clock signal, it can complete the transfer eight data.

### B. System Functional Description

The basic function of the system is shown in Figure 1. SPI interface chip interconnect mainly is constituted by four pins: SCK, MOSI, MISO and /CS. SCK is a common clock of across the SPI bus. MOSI, MISO is master and slave input and output machine logo pin. MOSI is the output pin of the master and input pin of the slave. MISO is the input pin of master and output pin of slave. /CS is a sign of the slave pin. In two SPI bus devices communicate with each other, /CS pin low level is a slave, on the contrary /CS pin high level is the master. In an SPI communication system, there must be a master. SPI bus can be configured as single-master and single-slave mode, single-master and more-slaves mode, each other master and slave mode.

Interconnection between two CPU uses SPI bus with exclusive signal line and the select signal line of chip. Speed of 10Mb / S's between the CPU is full-duplex communication. CPU can share access to external devices without conflict by exclusive signal line. Between the CPU can access the other CPU's memory, registers and equipment. At the same time it can send pre-defined action instructions to the other CPU.

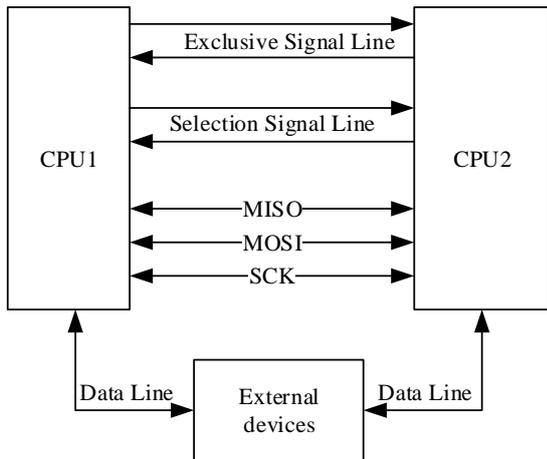


Figure 1. Multi-CPU interconnect design based on SPI bus

By sharing access to external devices such as Flash, so efficient external mass data access becomes possible. Traditional CPU interconnect massive data access methods is CPU1 sends commands to CPU2 then CPU2 reads the data and forwards it to CPU1. In this process, the developers need to weigh speed, buffer, data correctness and other issues which greatly limits the ability of CPU1 getting external mass data because of the limited memory space. However, after the adoption of the way now, for each CPU, external devices are independent of its services, read and write data without relying on any third-party device, but to solve the problem of conflict accessed through exclusive signal line. This design is the liberation of the difficulty of software development.

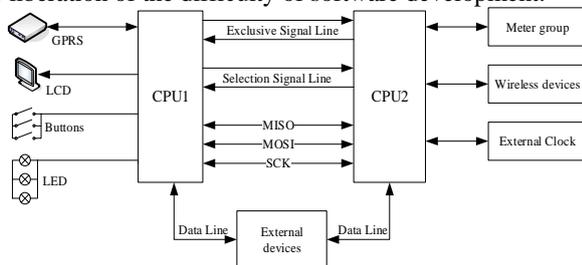


Figure 2. Charge collection terminal functional diagram of dual-CPU

### III. SYSTEM COMPONENTS

#### A. Block diagram of the system

Structure of the system diagram is shown in Figure 2. In the low-voltage electricity collection terminal, one CPU is responsible for upwards of data processing, transmission, key features, screen and another CPU is responsible for data collection and processing down. Multi-CPU applications is shortened the response time to be charged the low-voltage electricity collection terminal, improved the speed of data processing and transmission, rich functionality of the processor and extended the application. Modern is reached the advanced level of similar products. This is achieved good

economic and social benefits of commercial applications in products.

#### B. Concurrent strategy presentation

##### 1) Master-slave type parallel communication strategy

Based on the known characteristics of communication by SPI, between the CPU1 and CPU2 must work in one master-slave communication mode. CPU1 always works in the master communication mode and CPU2 has been working in the slave communication mode. All communication is initiated by CPU1, CPU2 passive response. Dual CPU work in RPC mode. RPC uses a client/server model. Requestor is a client and Service provider is a server. First, the client calls the process which sends a message to call the process parameters to the service process, and then waits for a reply message. On the server side, the process of maintaining sleep until the calling information arrived. When a calling message arrives, the server gets the process parameters, calculates results, sends a reply message then waits for the next call information. Finally, the client receives the reply message calling process, the process of obtaining and the results then calls the execution to proceed. Through RPC calls, we can be regarded CPU2 as a peripheral of CPU1, the CPU1 is for shielding the processing function of CPU2.

If CPU2 need to communication with CPU1, it should set signal line of selection to apply for a interrupt request. After establishing a data connection between CPU1 ,

CPU1 analysis the request content of CPU2 then respond to requests CPU2 to achieve a dual-processor direct parallel data transfer..

As CPU2 always works slave mode in this kind of mode, If you need to request saying only passively transmit data, real-time response is slow. But we found that in the majority of applications, the probability of CPU2 active uploaded data is very small, almost negligible after investigation. So this kind of model is still very wide range of applications

##### 2) Parallel Communications Strategy of exclusive master-slave flip-type

The main types of communication strategies used by the master-slaver communication mode which can flip. CPU1 and CPU2 is no strict definition master-slave relationship. When who will take time to communicate, it need to set up itself of the master communication terminal, then tells the other. So the other side will automatically work to the slaver communication terminal. Through RPC calls, we can directly access each other's registers and other information. For users, this is one processor working.

#### C. Functional description of each module

According to the site survey, we will set collection terminal dual-CPU system to work in a master-slave type parallel communication mode.

##### 1) CPU1 Function Description

CPU1 is mainly responsible for the upstream part of the acquisition of communication with the user terminal and the man-machine interface functions related to the operation. The user can use the buttons to set the rules for the functioning of the entire system. LED used to display the current operational

status of the collection terminal. Operation of the LCD screen can display the image of the entire system. CPU1 can interact with information through GPRS or RS485, and Ethernet and other ways with the main station. It is Responsible for the main station protocols between the analytical and structural. Through encryption and decryption operations, the scene data (meter data, real-time clock, etc.) is transmitted to the master station. The master station can also send commands to control under power collection terminal's work. Achieve power collection terminal through master online update feature and save a lot of manpower and material costs.

CPU1 is also responsible for implementing and coordinating the work of CPU2. Interact using RPC model for control and data CPU2 achieve CPU2 configuration and upgrade work.

### 2) CPU2 Functional Description

CPU2 main collection is done to the meter groups. Meter communication protocol is based on the completion of the field meter data acquisition and storage. Wireless communication may also be used the way the collected data to the remote meter terminal. The work may also be determined through the clock reference of the whole system real-time clock.

### 3) Mutually exclusive access to the external data source description

Traditional public external memory access method is generally used to achieve the dual-port RAM. CPU1 and CPU2 can simultaneously access a dual-port RAM chips. In this way, the system supports two CPU direct data exchange. Working principle is shown in Figure 3. A memory with two separate address, data and control lines so that allowing two independent CPU controller simultaneously or asynchronously access the storage unit. The main problem with this kind of access is the existence of that Dual-port RAM capacity are generally small, System design complexity and System more expensive.

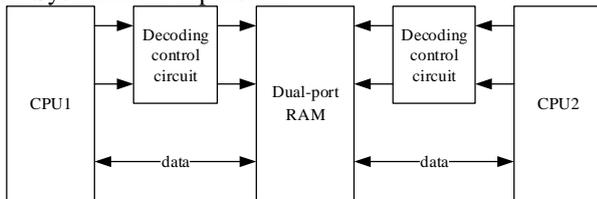


Figure 3. Dual-port RAM Working principle

Uses exclusive access to external data sources can be a better solution to the dual-port RAM access the problems.

Applicable under CPU1 and CPU2 access to external data memory is not very frequent. Exclusive signal line is used to arbitrate CPU1 and CPU2 who use external devices. CPU2 needs to be collected at the scene of the data stored in the external memory. The CPU1 needs to read data from external memory uploaded to the master station. It can effectively solve the problem of access to the conflict between the two signal lines through Exclusive Signal Line.

## IV. CONCLUSIONS

Popularity of computer applications and networks for embedded products created new and tremendous opportunities. Market demand for remote control devices is growing. The real-time and stability requirements of the system is increasing.

Concurrent real-time collection terminal system technology has been used in low-voltage electrical energy harvester remote meter reading system. The system is a good solution to the conflict with the substantial growth in electricity power enterprises understaffed. It is for power companies to save a lot of manpower and resources for power companies. The first line of skilled workers to copy from numerous annoying nuclear complex and other simple repetitive labor income freed, better maintenance and supply facilities into business expanding and other work. Better practice national grid company's proposed service requirements. In addition to the power system, security and surveillance in the area, industrial production line automation, aerospace and other fields, multi-machine parallel real-time collection terminal system also has broad application prospects.

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