Design of the Annular Pulse Generator Based on Quartus II

He Gu[1, a], Yefeng Chu[2, b]

[1]College of Computer Science and Technology, Changchun University,

Changchun, 130022, China

[2]College of Computer Science and Technology, Changchun University,

Changchun, 130022, China

[a]email:103471996@qq.com, [b]email: 191184698@qq.com

Keywords: Quartus II; Timing signal Simulation; Ring-Pulse

Abstract. In this paper, from the experimental teaching, to describe the process of timing signal produce in the micro-program controller, and using Altera Quartus Ⅱ that is integrated development platform to validation logic functions. By the simulation design, you can see the design effect visually, to get a ring-pulse in expected same as expected. Application of this method, making the effect of teaching more intuitive, it's a improvement for teaching of the hardware experimental.

Introduction

Development of computer technology is based on electronic technology, and development of hardware technology is it's precondition, in the teaching course, we want to show a more intuitive effect to the students, therefore, we introduce the Quartus II as simulation technology, simulate the logic functions of the circuit, make the theory and simulation combination closely, so can improve the students' interest in learning, strengthen ability of the students' hands-on and practical. To improve the quality of teaching effectively, will transform logic teaching abstractive into intuitive and visualization.

In the paper, we use the design of annular pulse generator as an example, to introduce the application of the Quartus II.

Quartus II Software is Introduced

Quartus Ⅱ is the Altera company develop the programmable logic design software in windows environment. It's a PLD/FPGA developed software that comprehensive and powerful [1].Quartus Ⅱ support principle diagram, VHDL, Verilog HDL and AHDL (Altera Hardware Description Language), and other forms of input. The logic function can be described directly used the above methods for testing simulation. In order to understand the function of realization is the original design requirements or not. The interface of this software has strong openness, after the compiler by the system editor, comprehensive operation and so on. The design of digital circuit to realize synchronous simulation analysis, time delay analysis, compile operations and so on, in the end, the circuit that can be compiled will allocation into one or more devices.

In addition, Quartus II used DSP and Builder as tools combined with the Matlab/Simulink, you can easily achieve a variety of DSP application system. Support programmable system development on the Altera chip. It is a comprehensive development platform that can make system design, embedded software development, and programmable logic design as whole.

The Timing Control Signal

As everyone knows, the core components of a computer system is the central processor unit, that is what we usually say CPU.CPU is made of the arithmetic unit, a controller and a register group. These parts can help the computer to complete the instruction control accurately, operation control, time control and data processing etc. The time control is an important condition to provide accurately, rapidly, in good order and arranged work well for computer.

Time control is generated by a timing signal generator. Once the machine is started, that is to say CPU began to taking instruction and instruction is executed. The operation controller used a timing pulse sequence and different pulse interval. Command the machine to work organized and rhythmically, what will do in this pulse arrival, what will do when that pulse comes, provide the time mark for each part of the computer while it's at work.

Timing signal generating circuit of a variety of computer is not the same. Speaking generally, The timing circuit is more complex for large and medium scale computers, the timing circuit is relatively simple for small and micro computers. This is because the former is more action, the latter involves the action of less. In the computer, the beat potential represents a CPU cycle time, a CPU cycle is divided into several smaller intervals by the clock pulse. With all these beats, computer can do the standard operation under the control of timing.

The Use of Quartus II Complete the Design Process of the Pulse Generator

(1)The ring pulse generator

The effect of annular pulse generator is to produce pulse sequence orderly, the time interval is equal or not equal, in order to produce the pulse beat ultimately required through the decoding circuit.

In this design, we assume that a CPU cycle can produce beat pulse in the same time period,T_1°-T_4°,each rhythm of the pulse width is 200ns,so a CPU cycle width is 800ns.In the next CPU cycle, they are repeated in a fixed time interval. As shown in Figure 1.The realization of the design using four D flip flops and some logic gates, the CLK as the clock signal input source， T1, T2, T3, T4 as the output signal, the purpose of design the purpose of design is to get to the ring pulse at the output port.

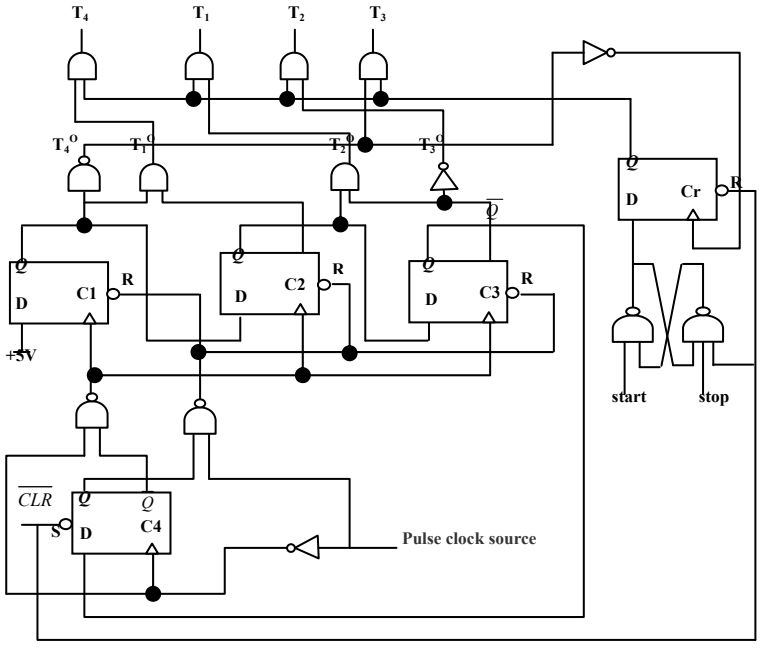

Figure.1.The logical structure of the ring pulse generator

According to the output logic circuit we can get the corresponding logical expressions:

$$T_1^O = C_1 \bullet \overline{C}_2 \quad (1)$$

$$T_2^O = C_2 \bullet \overline{C}_3 \quad (2)$$

$$T_3^O = C_3 \quad (3)$$

$$T_4^O = \overline{C}_1 \quad (4)$$

The analysis of the working process in each D flip flop,where C_4 is the control terminal can reset the whole system. After the start of the circuit, the States of C_4, C_3, C_2, C_1 can decide the states of theT_1^O,T_2^O,T_3^O,T_4^O.Start and stop circuit can produce the output states-T_1, T_2, T_3, T_4.

The circuit design needs to get a beat continuously. Such as shown in Figure 2.According to the logical expression of the T_1,T_2,T_3,T_4,we can know the rhythm potentials are realized.

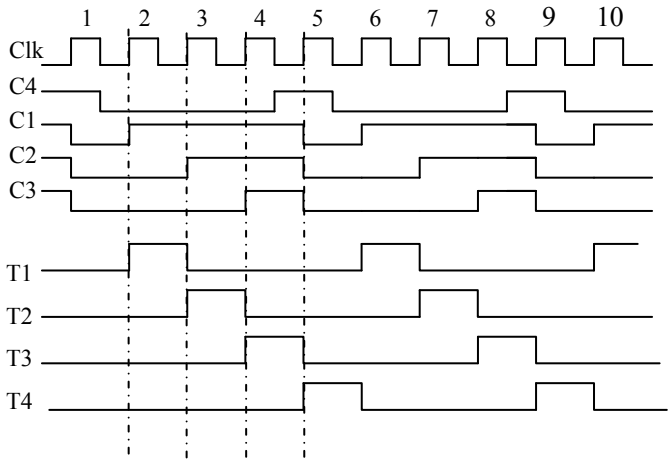

Figure. 2. Relationship between rhythm potential and rhythm pulse

Among them, rhythms-T_1, T_2, T_3, T_4 is the computer need at work. The width of the beat pulse depend on the input clock frequency source. The input clock source provides the clock signal frequency, and provide clock pulse signal that the electrical signal matched. It is usually consists of positive feedback oscillation circuit that be made of clock crystal oscillator and NAND gate, its output is sent to the ring pulse generator.

(2) Using Quartus II to complete the circuit design

① Set up and compile of new file

Start quartus II, in the main menu, used File-New-Block Diagram/Schematic File, create a new file, and with. gdf as it's extension. Enter the blank editing interface, on this interface, find the path of basic component library using the symbol window. Find the logic device from the device database, complete the circuit connection, as shown in figure 3.

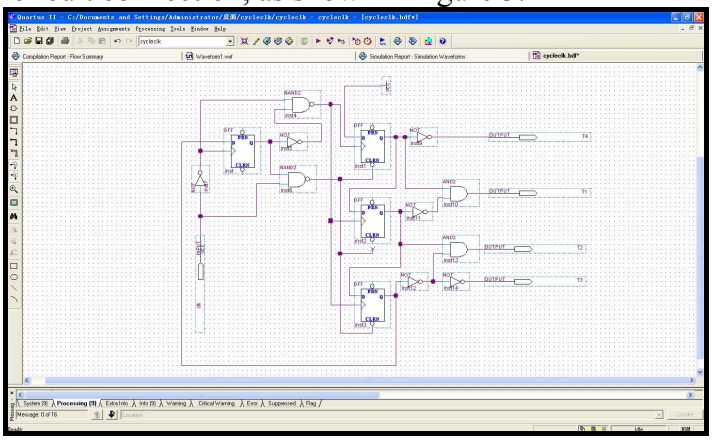

Figure.3.Schematic diagram of the circuit

After the completion of the circuit drawing, change the name of the input pin and output pin. The input pin is defined as "CLK", the output pin is defined as T_1, T_2, T_3, T_4. Select "Fil e-save as" in the main menu, and input the file name, at the same time, select "File-Project-Name", and input file name with the same project name, after same. Compile completely to th

e circuit by “Processing-start compilation”.In the process of compiling,pay attention to the co mpile information in the bar of the “Processing” under the project management window, ch eck and correct errors, until compile success.

② Simulation timing waveform

Open the waveform editor by “File-New-Vector Waveform File”, set up a new wave file that the expanded-name is .SCF. Select end time in the Edit menu, in the “Time bar” within the pop-up window, set the simulation time is 50μs during the whole regional. List the input signal-Clk and the output signal - T_1,T_2,T_3,T_4 by “Node Finder". And assignment to the input pin. The signal input can be electrical level can also be a pulse mode, in this case, only one input pin, it is Clk, and the input signal is pulse input. The pulse width of input clock signal is 100ns in the Clk pin. As shown in figure 4.

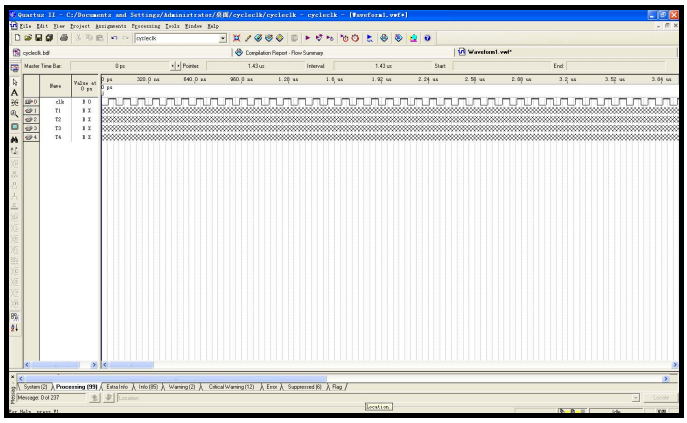

Figure .4.Node selection and input signal set

Save the file and start to compile. Because of the delay of the transmission device, Quartus II provides timing simulation and functional simulation. It is clear to see the influence on output pin by time delay, as shown in figure 5.

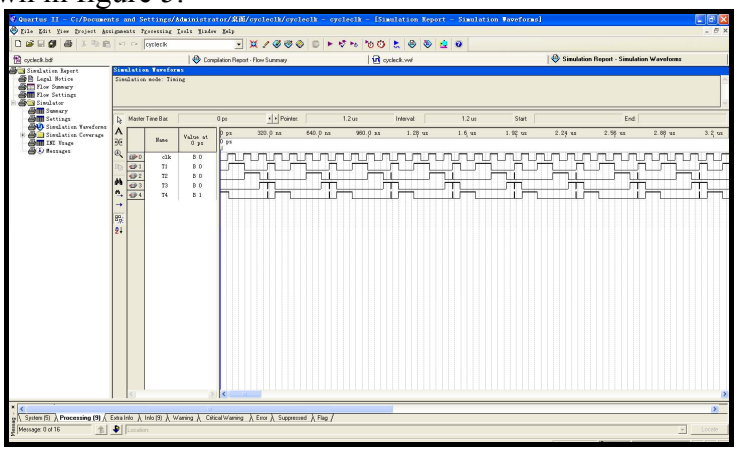

Figure.5.The simulation model with time delay of the ring pulse

In order to see the effect of figure better, we can choose the function simulation, we need to use simulation tools “Simulator tool”, and change the simulation mode into “Functional”, at this time the waveform ignore delay. As shown in figure 6.

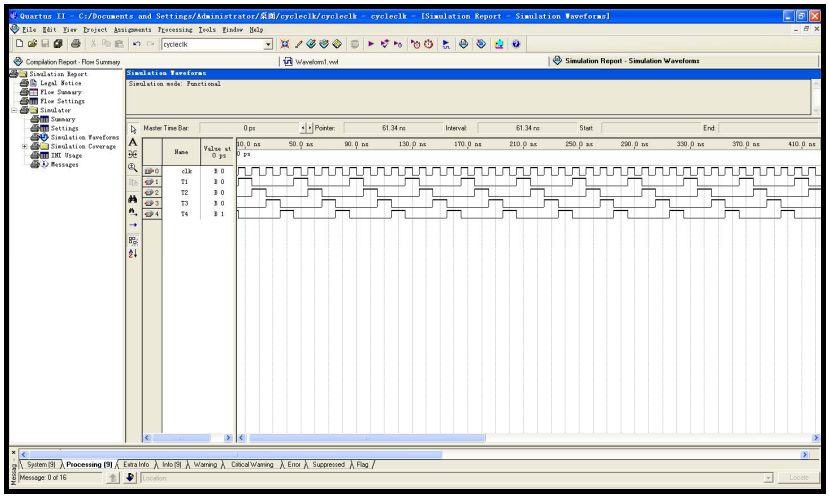

Fig.6. Functional simulation of pulse waveform

Through the simulation waveform can be very intuitive to see the timing is exactly what we expect to get results. In the design we can change the pulse width of CLK to get a different beat cycle of potentials.

Conclusion

The Quartus II simulation software is introduced in the teaching, can make the theory teaching more intuitive. Deepen students understanding for courses. By using the auxiliary design of the software, let the students starting from the basic logic circuit design, through the simulation results understand the different characteristics of the basic circuit, deepening the understanding of the structure of computer organization. The whole design process can make the teaching and experimental verification executive at the same time, and can display the abstract theoretical knowledge with the scientific and intuitive way, to get good results on the cultivation of practice ability.

Reference

[1] Liqiang Niu, Ning Xu.The application of Quartus II software in FPGA technology in Teaching. Sciences and Technology Information. 2011. 36.

[2] Song Pan, Ming Pan. Modern computer principle. Science Press. In February 2007 .first edition

[3] Zhongying Bai, Computer composition principle, Science press, In November 2001, third edition

[4] Hui Wang.Max+plus II and Quartus II application and development skills. Machinery Industry Press, In 2007 March. the first edition

[5] Yuanfang Xin.The application of Quartus II simulation technology in Teaching.The development of economy and science and technology information, In 2007 seventeenth Volume 32