Research on the structure and configuration of MCU clock system for Kinets series

WangJing[1, a], WangZhenchong[1, a]

[1]China University of Mining &Technology, Beijing, Beijing, China

[a]email: wangjing_kd@163.com

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Abstract. Kinetis L-series MUC clock system includes the clock source mechanisms such as the internal reference clock source, frequency-locked loop FLL, oscillator OSC, real time clock RTC, and provides many clock models to provide technology foundations to many low power applications, and has the features such as low power consumption, multifunction, and high performance. By the analysis of K60 clock system working mechanism, test of the clock and focusing on the analysis of the operation mechanism of the multifunctional clock generator, and puts forward the test methods of clock source performances required during the relevant chip application and design process of Kinetis and the select methods of clock sources of each functional module of the chip systems.

Introduction

K60 was officially launched by Freescale company in 2010, and it adopted MCU of Kinetis-series of ARM®CortexTM-M4 core, and had the features of low power consumption, high performances and multifunction. It helps to improve the instantaneity and stability of the embedded system and reduce the power consumption of the system to allocate correctly and reasonably choose the clocks. At the present, there are many researches on reducing the power consumption of the embedded system by the clock mechanisms. Hereafter it will take the K60 as an example to analyze the structures and operation mechanisms of the systems of Kinetis-series MCU clocks, and give the selective basis and allocation methods of the internal and external reference clocks, and analyze the features of each operation model of MCG modules and the transport process of the model status, and finally put forward the analysis methods of each clock source performances and conclude the selective and allocation methods of the system modules to the clock sources.

Freescale Kinetis-series K60 Clock System

Freescale K60 clock system.

Freescale Kinetis-series is a micro-controller launched by Freescale basing on the core of ARM CORTEX-M4

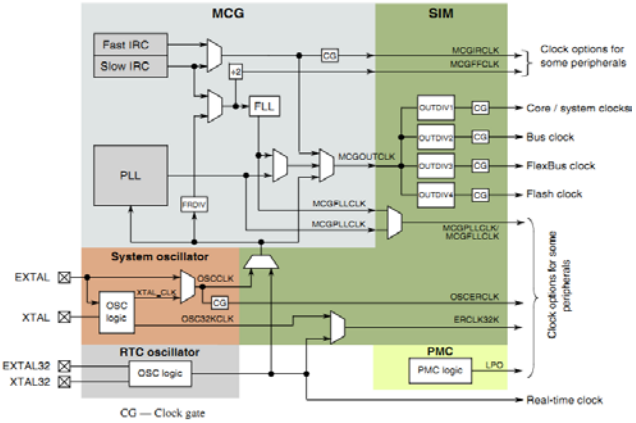


Fig.1. K60 clock system

Freescale K60 clock system is as shown in the above figure, and it can be seen that there are four source clocks of the device.

(1) The internal reference clock source includes Fast IRC and slow IRC (IRC-International Reference Clock)

(2) The external reference clock source only has an EXTAL base pin as the clock input, and it can be realized by using active crystal oscillator.

(3) The external crystal resonator uses two base pins of EXTAL and XTAL for the input

(4) The external 32K RTC resonator is used for the clock input of the real-time clock

It can be seen from the figure that in order to provide clock signals to the system, it is crucial to generate MCGOUTCLK output at last. And MCGOUTCLK, then by the frequency division can provide Core/system clocks、Bus clock、FlexBus clock and Flash clock. There are 3 methods for the generation of MCGOUTCLK:

①Provided directly by the internal reference clock source IRC, and this clock source is integrated within the chips (including the Slow IRC) with the frequency of 2M

②Provided by FLL or PLL modules.

③Provided directly by the external clock, including the external reference clock source (one base pin input), the external crystal senator is output through the XTAL_CLK and RTC OSC logic clocks generated by the internal OSC logic.

Generally speaking, MCGOUTCLK is produced by PLL or FLL frequency multiplication, and the official routine of Freescale is finally provided by PLL module. From this figure it can be seen that the clock input of PLL module is OSCCLK or RTC OSC logic. My plate provides PLL clock by the external reference clock source, and finally produces MCGOUTCLK through PLL， that is EXTAL-->PLL module -->MCGOUTCLK

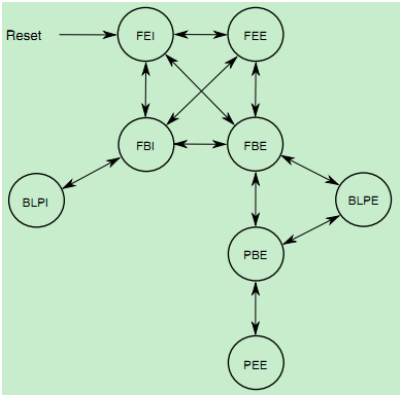


Fig.2.

From the figure it can be seen that this chip includes 8 working clock modules pluse Stop module. The system enters the default FEI module directly after being RESET. In this figure, F—FLL, P—PLL, E—Enable or EXTAL , B—Bypass, I—Internal, L—Low Power

FLL starts, internal reference clock (FEI), clock provided FLL by the internal reference clock, FLL drives MCGOUT.

FLL starts, external reference clock (FEE), clock provided FLL by the external reference clock, FLL drives MCGOUT

FLL Bypass, internal reference clock (FBI), MCGOUT is driven by the internal reference clock even FLL is operating

FLL Bypass, external reference clock, MCGOUT is driven by the external reference clock even FLL is operating

PLL Bypass, Bypass, external reference clock （PBE）, MCGOUT is driven by the external reference clock even PLL is operating

PLL starts, external reference clock (PEE), clock provided PLL by the external reference clock, PLL drives MCGOUT

Both BLPI FLL and PLL are forbidden, internal clock reference source drives MCGOUT

Both BLPI FLL and PLL are forbidden, external clock reference source drives MCGOUT

As the system enters the fault FEI mode, and our target is to jump to PEE model hence it will refer to the conversion of mode. In this figure, it can't directly jump from FEI to PEE and it must be conversed via the other modes.

Clock System Allocation

Selections of the internal and external reference clocks.

MCG _C1[CLKS] is used to select the internal and external reference clock sources, CLKS=01, select the internal reference clock, and CLKS=10, select the external reference clock; MCG_C2[IRCS] is used to select the fast and slow internal reference clocks, IRCS=0, select the slow internal reference clock 32K crystal oscillator, IRCS=1, select the fast internal reference clock 4M crystal oscillator; SIM_SOPT2[MCGCLKSEL] is used to select the external reference clock, and MCGCLKSEL=0, select the systematic oscillator OSC, MCGCLKSEL=1, select the real time clock oscillator RTC OSC.

Selections of phase-locked loop and frequency-locked loop.

MCG _C6[PLLS] is used to select phase-locked loop FLL and frequency-locked loop PLL, PLLS=0, select FLL，PLLS=1, select PLL. MCG_C1[FRDIV] is the external reference clock frequency division factor of FLL, and jointly determine the value range from 1 to 1024 with MCG_C2[RANGE]; and MCG_C5[PRDIV] is the external reference clock frequency division factor of PLL, and the value range is from 1 to 25; MCG_C6[VDIV] is the frequency multiplication factor of PLL voltage control crystal oscillator, and the value range is from 24 to 55.

Analysis of MCG Operational Mechanism

Operational mode of MCG clock.

The clock operational mode is defined and classified according to the working conditions of FLL or PLL of MCG, the selected clock and whether the output clock provides .MCGOUTCLK. For example, when PLL is working, the external reference clock shall be selected and the frequency-locked clock MCGPLLCLK shall be provided to MCGOUTCLK, and meanwhile, MCG clock mode is called PEE (PLL external busy); and if the clock output by PLL does not provide MCGOUTCLK, but being sent to MCGOUTCLK by the external reference clock OSCCLK, at this time, MCG clock mode is called PBE (PLL external bypass), and the rest can be done in the same manners. There are 9 clock operational modes of MCG: FEI，FEE，FBI，FBE，PBE，PEE，PEE，BLPI，BLPE and STOP, the mode shift shall be complied with the MCG shift rules shown in figure 2, and any status in this figure can be shifted to STOP, and the arrows in the figure indicate the allowed MCG mode shift directions. 9 clock operational modes can be divided into 4 working modes, namely, initial status: the initial status after restart, intermediate status: MCGOUTCLK clock sources provided not by FLL/PLL output, but by the corresponding reference clocks, working status: MCGOUTCLK clock sources are provided by FLL/PLL output during the normal operation, and by the internal and external reference clocks at low power consumption, stopped status: MCG stops working, table 1 gives the relationships between all modes and working status[10].

Tab.1. Relationships between clock operational mode and working status

working condition	Clock operational modes	Reference clocks	MCGOUTCLK clock sources
initial state	FLL internal busy	32KHz IRC	MCGFLLCLK（20~96MHz）
Intermediate status	FLL external bypass	Fractional frequency of OSCCLK 31.25~39.0625KHz	Frequency of external crystal oscillator
	FBI	32KHz IRC	IRC（31.25KHz~4MHz）
	PBE PLL external bypass	Fractional frequency of OSCCLK 2 MHz ~4MHz	Frequency of external crystal oscillator

Working status	PLL external busy	Fractional frequency of OSCCLK 2 MHz ~4MHz	MCGPLLCLK（48~100MHz）
	Low power consumption internal bypass	32KHz IRC	32KHz or 4MHz
	Low power consumption external bypass	Fractional frequency of OSCCLK 2 MHz ~4MHz	Frequency of external crystal oscillator
	FLL external busy	Fractional frequency of OSCCLK 31.25~39.0625KHz	MCGFLLCLK（20~96MHz）
Stopped status	Stopped mode	After MCU enters STOP mode, MCG also stops working.	

Tab.2. Recommended values of clock allocations

clock	Frequency
Core clock/system clock	96 MHz
Bus clock	48 MHz
FlexBus clock	48 MHz
Flash clock	24 MHz

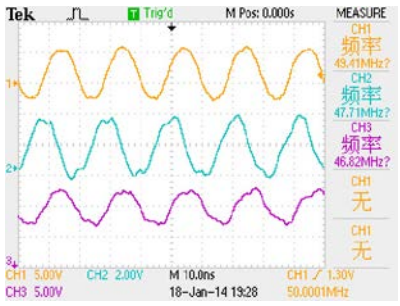
Analysis of the Clock Source Performances

Measuring methods of clock source frequency.

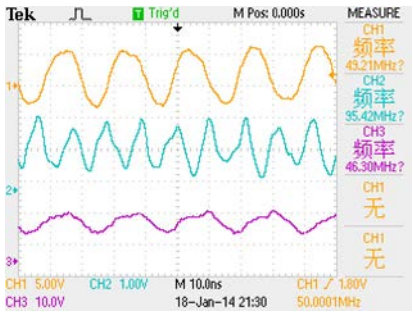
The external reference clock can directly measure the external access pins of XTAL and XTAL32; in K60 chips, PTA6 can be allocated as TRACE_CLKOUT and the functions can be used to output the current clock MCGOUTCLK and core clock Core/System CLK; FlexBus clock can allocate PTC3 as FB CLKOUT output, and RTC real time clock RTCCLK can allocate PTE26 as RTC_CLKOUT output. In the MCU chips of Kinetis –series, PTC3 can be allocated as CLKOUT function in order to output the bus clock Bus Clock、LPO, internal reference clock MCGIRCLK, external reference clock OSCERCLK; the output function of RTC_CLKOUT can be realized by allocating PTE0.

Experiment data analysis.

The experiment data is finished on the SD-FSL-K60-C evaluation board of Suzhou University Freescale Embedded Center by using TEK TDS2024B oscilloscope. In this experiment, channel 1 (CH1) measures the external reference input ETAL, and channel 2 allocates TRACE_CLKOUT into MCGOUTCLK and Core/System CLK by using SIM_SOPT2[TRACECLKSEL, and channel 3 measures the system FlexBus signals FB_CLK,, in figure 4, the external reference clock 50MHz, MCGOUTCLK taking PLL as the clock source with the allocation of 96MHz,MCGOUTCLK:Core/SystemCLK:BusCLK:FlexBus:FlashBus=4:2:2:2:1;in figure 5, the external reference clock 50MHz,MCGOUTCLK, taking PLL as the clock source with the allocation of 192.3MHz,MCGOUTCLK:Core/SystemCLK:BusCLK:FlexBus:FlashBus=4:2:2:2:1.



Frequency None
Theoretical value 50MHz
Theoretical value 48MHz
Theoretical value 48MHz
FB_CLK=Core/System CLK/2
Figure 4 test data of clock source 1



Frequency None
Theoretical value 50MHz
Theoretical value 96MHz
Theoretical value 48MHz
FB_CLK=MCGOUTCLK /4
Figure 5 test data of clock source 2

Fig.3.

Conclusion

The clock system so Kinetis-series MCU can insert the frequency signal sources through the internal and external reference clocks, and provides many clock sources by the multifunctional clock generator MCG to each functional module, and uses the functional module clock of the clock gate module start/stop systems and the clock allocation mechanism to choose the lower working frequency for each functional module under the premise of meeting all requirements in order to ensure that it can stabilize the works at a low power consumption. The problems such as the migration selection on MCG operation mode and the relationships between the effectiveness of clocks and the power modes (namely the lower power consumption mode) will be further analyzed and researched in the subsequent works.

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