

An Algorithm on Direct Tunneling Current Model Based on DIBL Effect

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Abstract—With the scaling of NMOS devices, gate tunneling current increases significantly under Drain Induced Barrier Lowering (DIBL), and static characteristics of devices and circuit are severely affected by the presence of gate tunneling currents. In this paper, a novel theory on direct tunneling current predicting model under DIBL is presented in ultra-thin gate oxide NMOS devices that tunneling current changes with gate-oxide thickness. To analyze quantitatively the behaviors of scaled MOS devices in the effects of gate tunneling current and predict the trends, the characteristics of NMOS devices are studied in detail using HSPICE simulator. The simulation results in BSIM4 model well agree with the model proposed. The theory and experiment data are contributed to the VLSI circuit design in the future.

Keywords- Scaled Device; Ultra-Thin Gate Oxide; DIBL; Direct Tunneling Current Model; Static Characteristics

I. INTRODUCTION

The size of MOS transistors has reached the point where gate tunneling currents become more important due to the reduced gate dielectric thickness [1]. Aggressive scaling of MOS devices requires use of ultra-thin gate oxides to maintain a reasonable short channel effect [2]. ITRS predicts gate-oxide thicknesses less than 1.4 nm for sub-100-nm CMOS which results in considerable direct tunneling current [3, 4]. For CMOS devices with thinner oxides, the gate-to-channel tunneling current becomes appreciable and dominates the total static state leakage of the transistor [5]. It is clear from the literatures that gate tunneling has been extensively modeled but some studies focused mainly on the theory of tunneling and the equations developed were not suitable for predicting behavior and trends by simulation due to their complexity [6, 7]. Also, assumptions such as ignoring tunneling in the PMOSFET and tunneling in the gate overlap regions were made [8, 9].

In this paper, following a double integral approach, a gate tunneling current model that reveals the relations between gate tunneling current and oxide thickness is

proposed, and the impact of gate tunneling current on current source inverter for future technology generations are studied in detail. Considering the tunneling of the NMOSFET in the gate and the gate-overlap regions, the degradation is simulated in characteristics of MOS devices and static current source inverter circuit due to gate tunneling currents across ITRS technology generations including 0.5~1.3nm oxide thickness corresponding to 25~90nm technology nodes, respectively. The degradation of inverter in performance is measured in terms of output voltage swing and power consumption. The effect of technology scaling on gate tunneling current is determined. All device parameters are changed appropriately when the oxide thickness is scaled and hence the effect of the variation of other parameters such as device doping concentration and oxide thickness are considered in the simulations. The results of simulation will be instrumental and provide the basis for designing circuit.

II. DIBL EFFECT

Drain Induced Barrier Lowering Effect is an important physical effect in VLSI device, and it is a limit in device applications. So, it is important for computing leakage current that build a tunneling current model considering DIBL effect.

Under the DIBL effect, threshold voltage ($V_{TH,D}$) can be expressed as equation (1) [10], and in equation (2), ΔV_{TH} is the change of threshold voltage considering DIBL effect.

$$V_{TH,D} = V_{TH} + \Delta V_{TH} \quad (1)$$

$$\Delta V_{TH} = \frac{-0.5}{\cosh(K \cdot \frac{L_{eff}}{l_{t0}}) - 1} (m_1 + m_2 \cdot V_{BS}) \cdot V_{DS} \quad (2)$$

In equation (2), L_{eff} is active length, l_{t0} and X_{dep0} can be obtained by equation (3) and (4), K is a gate dielectric constant (3.9), m_1 and m_2 are the process parameters obtained by parameters extraction, X_{dep0} is the depletion layer edges while $V_{BS}=0$, n_d is doping concentration

($1.7 \times 10^{17} \text{cm}^{-3}$), n_i is carrier concentration, ϵ_{Si} is dielectric constant of Si and ϕ_s is surface potential.

$$l_{T0} = \sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}} \quad (3)$$

$$X_{\text{dep}0} = \sqrt{\frac{2\epsilon_{\text{Si}}\phi_s}{qn_d}} \quad (4)$$

The surface potential ϕ_s is shown in equation (5), k is Boltzmann constant, q is electronic charge (1.6×10^{-19}), T is absolute temperature, and $PHIN$ is shown in equation (6).

$$\phi_s = 0.4 + \frac{kT}{q} \ln\left(\frac{n_d}{n_i}\right) + PHIN \quad (5)$$

$$PHIN = -qD / \epsilon_{\text{Si}} \quad (6)$$

While substrate bias $V_{BS}=0$, as $\phi_s = \phi_s + V_{BS}$, the potential ϕ_s is

$$\phi_s = \phi_s = 0.4 + \frac{kT}{q} \ln\left(\frac{n_d}{n_i}\right) \quad (7)$$

III. GATE DIRECT TUNNELING CURRENT MODEL

As illustrated in Fig. 1, the gate tunneling current is composed of several components. I_{gso} and I_{gdo} are parasitic leakage currents through gate-to-S/D extension overlap region; and I_{gc} is the gate-to-inverted channel tunneling current. Part of I_{gc} is collected by the source (I_{gs}) while the rest goes to the drain (I_{gd}) [11,12]. Considering overall leakage currents, the relation between direct tunneling current and dielectric thickness is studied in detail. So the tunneling current density according to the BSIM4 transistor model [10] is

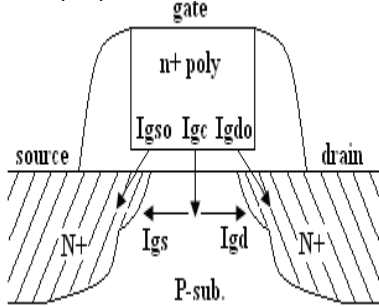


Figure 1 Components of tunneling

$$J_{DT} = J_G = AE_{\text{ox}}^2 \cdot \exp\left[BE_{\text{ox}}^1 \left(1 - \left(1 - \frac{V_{\text{ox}}}{\phi_{\text{ox}}}\right)^2\right)\right] \quad (8)$$

By $1 - \left(1 - \frac{V_{\text{ox}}}{\phi_{\text{ox}}}\right)^2 \approx 1$, the tunneling current at point x can be approximated as

$$J_G(x) \approx AE_{\text{ox}}^2 e^{-B/E_{\text{ox}}} \approx AE_{\text{ox}}^2 e^{-B/T_{\text{ox}}(V_{\text{ox}} - V(x))} \equiv J_{G0} e^{-B^*V(x)} \quad (9)$$

Where T_{ox} is oxide thickness, J_{G0} the gate tunneling current density ($V_{DS}=0$), $V_{\text{ox}} \approx V_{GS}$ the gate-source voltage at point $x=0$, $B^* = pBX_{\text{ox}} / V_{\text{ox}}^2$. If the gate leakage current is much smaller than drain current, then

$$V(x) = V_{GS} - V_{THD} - \sqrt{(V_{GS} - V_{THD})^2 - 2(V_{GS} - V_{THD} - V_{DS}/2)V_{DS} \cdot x/L} \quad (10)$$

$$\approx (V_{GS} - V_{THD} - V_{DS}/2) \cdot V_{DS} / (V_{GS} - V_{THD}) L \cdot x$$

The total gate tunneling current is expressed as

$$I_G = W \int_0^L J_G(x) dx = (WL) \cdot \frac{\int_0^L J_G(x) dx}{\int_0^L dx} = (WL) \langle J_G(x) \rangle \quad (11)$$

Where $J_G(x) = J_{G0} e^{-B^*V(x)}$ is the gate tunneling current density at point x .

From the equations (2) 、 (3) 、 (4) and $I_G = W \int_0^L J_G(x) dx$, $k = (V_{GS} - V_{TH} - V_{DS}/2) V_{DS} / (V_{GS} - V_{TH}) L$, $B^*k = p$, the gate tunneling current is

$$I_G = W \int_0^L J_{G0} e^{px} dx = J_{G0} W \frac{1}{p} (e^{pL} - 1) = \frac{J_{G0} W}{p} e^{pL} - \frac{J_{G0} W}{p} \\ = \frac{J_{G0} WL (V_{THD} - V_{GS})}{B^* [(V_{GS} - V_{THD}) V_{DS} - V_{DS}^2 / 2]} \exp\left(\frac{-B^* V_{DS} (V_{GS} - V_{THD} - V_{DS} / 2)}{V_{GS} - V_{THD}}\right) \\ + \frac{J_{G0} WL (V_{GS} - V_{THD})}{B^* [(V_{GS} - V_{THD}) V_{DS} - V_{DS}^2 / 2]} \quad (12)$$

Model (12) can be simplified as

$$I_G = \frac{J_{G0} WL (V_{THD} - V_{GS})}{B^* [(V_{GS} - V_{THD}) V_{DS} - V_{DS}^2 / 2]} e^{-B^* / C} + J_{G0} WLC / B^* \quad (13)$$

In this case $V_{BS}=0$, the change of threshold voltage ΔV_{TH} is

$$\Delta V_{TH} = \frac{-0.5m_3 V_{DS}}{\cosh(m_3 \frac{L_{\text{eff}}}{l_{T0}}) - 1} = \frac{1}{2} m_3 V_{DS} \frac{1}{\cosh\left(\frac{m_3 L_{\text{eff}}}{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}\right) - 1} \quad (14)$$

m_3 is process parameter from parameter extraction, and $\cosh(x) = (e^x + e^{-x})/2$, then

$$\Delta V_{TH} = \frac{V_{DS} m_3}{1 - e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}} - e^{-\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}} = \frac{V_{DS} m_3}{1 - K_1 e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}} \quad (15)$$

Since, Equation (16), (17) and (18), the direct tunneling current mode of scaled device under DIBL effect is given by equation (19).

$$K_1 = e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}} + e^{-\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}} \quad (16)$$

$$\frac{C}{B^*} = \frac{1}{T_{\text{ox}}} \frac{V_{GS}^2}{pB} \frac{V_{GS} - V_{TH} - \frac{V_{DS} m_3}{1 - K_1 e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}}}{(V_{GS} - V_{TH} - \frac{V_{DS} m_3}{1 - K_1 e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}) V_{DS} - \frac{1}{2} V_{DS}^2} \quad (17)$$

$$\frac{-B^*}{C} = T_{\text{ox}} \frac{pB V_{DS}}{V_{GS}^2} \left(1 - \frac{V_{DS}}{2V_{TH} + \Delta V_{TH} - V_{GS}}\right) = T_{\text{ox}} \cdot K_2 \left(1 - \frac{V_{DS}}{2V_{TH} + \Delta V_{TH} - V_{GS}}\right) \quad (18)$$

$$I_G = J_{G0} W \frac{C}{B^*} (1 - e^{-B^* / C}) \quad (19)$$

$$= J_{G0} W \frac{1}{T_{\text{ox}}} \frac{V_{GS}^2}{pB} \frac{V_{GS} - V_{TH} - \frac{V_{DS} m_3}{1 - K_1 e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}}}{(V_{GS} - V_{TH} - \frac{V_{DS} m_3}{1 - K_1 e^{\sqrt{\frac{\epsilon_{\text{Si}} T_{\text{ox}} X_{\text{dep}0}}{K}}}) V_{DS} - \frac{1}{2} V_{DS}^2} \left[1 - \exp\left(-T_{\text{ox}} K_2 \left(1 - \frac{V_{DS}}{2V_{TH} + \Delta V_{TH} - V_{GS}}\right)\right)\right]$$

IV. OFF-STATE CHARACTERISTICS SIMULATION

Based on the BSIM4 model, the trends in the gate currents of NMOSFET across technology generations were simulated for different bias conditions. These simulations were carried out in HSPICE. Table 1 shows Structure Parameters of device, and the results plotted in Figs. 2, 3, 4 for NMOSFET. In Figure 2, the NMOSFET is biased with $V_{GS,N}=0$, $V_{DS,N}=0\sim V_{DD}$ in the cut-off range. It is found that the thinner the thickness of oxide layer, the faster the increase of gate tunneling current. With the reduction of the thickness of gate oxide layer, the gate tunneling current increases by three orders of magnitude from 10^{-9} (A) to 10^{-6} (A). In Figure 3, the NMOSFET is biased with $V_{GS,N}=0\sim V_{DD}$, $V_{DS,N}=0$ in the cut-off range considering DIBL effect. It is found that the gate tunneling current is bigger.

Fig. 2~3 highlights that the gate tunneling current increase with the reduction of the thickness of gate oxide layer. To further illustrate the functional form of gate tunneling current increases, it will be explained through Fig. 4. In Figure 4, the simulation results and theoretical results are given. The results show that the simulation results are consistent with theoretical results.

TABLE I DEVICE STRUCTURE PARAMETERS FOR SIMULATION

Parameters	Values					
Gate length(nm)	90	75	65	53	45	40
Channel length(nm)	65	53	45	37	32	28
Overlapping area length(nm)	12.5	11.0	10.0	8.0	6.5	6.0
Oxide layer thickness(nm)	1.3	1.2	1.1	0.9	0.8	0.7
Supply voltage(V)	1.2	1.1	1.0	1.0	0.9	0.9
Threshold voltage(V)	0.35	0.33	0.32	0.30	0.28	0.27
Junction depth(nm)	71.5	58.5	49.5	36.0	35.5	31.5
Substrate doping concentration(10^{19}cm^{-3})	0.4	0.6	0.8	1.1	1.4	1.6
Channel doping concentration(10^{18}cm^{-3})	1.15	1.15	2.0	2.0	2.0	3.0
Gate doping concentration (10^{20}cm^{-3})	0.92	0.92	1.14	1.5	1.66	1.66

V. SUMMARY

In this paper, the theoretical model of the relationship on DIBL effect between gate tunneling current and the thickness of gate oxide layer is deduced according to the physical mechanism of tunneling. These simulations were carried out in HSPICE based on BSIM4 parameters. The gate tunneling currents are studied quantitatively by different cut-off range with insulating layer SiO_2 . In addition, the comparison without DIBL effect is made. For NMOSFET devices, the simulation results agree with the theory model proposed. The gate tunneling current exponentially increase with gate oxide thickness decreases.

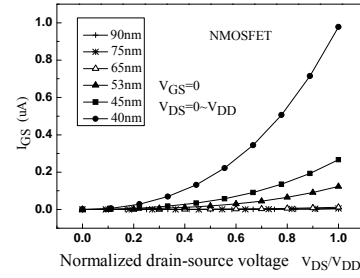


Figure 2 Gate Current $V_{GS}=0$

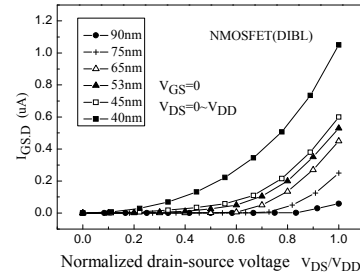


Figure 3 Gate Current under DIBL Effect $V_{GS}=0$

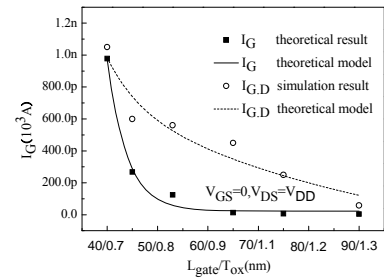


Figure 4 Comparing of Tunneling Current trends

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