The Design and Implementation of Improved MPSK Modulator with Signal Recognition Based on FPGA

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Abstract—MPSK is a modulation method which uses various phase states of the carrier to describe digital information. And it is widely used in the field of digital communications. Now, the applicable scope of MPSK signal modulation is too narrow, and it is necessary to know the type of signal source to modulate in advance, which have limit the development of MPSK. In this paper, we use the identification algorithm of time and frequency overlap signals in single-channel to differentiate and modulate the type of MPSK signals. This design improves the applicability and operability of the modulator. At the end of this paper, we merge all the modules to implement the MPSK signal modulator with the function of signal sort recognition. This design uses the hardware description language VHDL to program, Quartus II 8.0 to integrate andwire, and ModelSim platform to simulate. Besides, MPSK modulator based on FPGA has a good practical application.

Keyword-FPGA; MPSK; time and frequency overlap; signal classification

I. INTRODUCTION

Signal modulation takes an important role in the area of computer networksand communication. MPSK (multiplephase shift keying) also called the numbersystem, is a multi-system digital phase modulation, which is the promotion of the modulation in binary. 4PSK(QPSK) and 4DPSK (QDPSK) are widely used during the M-system modulation of digital phase[1]. The 3G mode in Chinaalso uses QPSK modulation in the down-link[2].

Now, there has beenmuch literature putting forward the design idea and algorithm of MPSK signal recognition and MPSK modulator[3,4]. However, the related designs are studied as independent modules, which make the mixing process too fragmented and thepromotion of MPSK modulation unconducive.

The design of MPSK modulator uses FPGA technology with the identificationalgorithm of time and frequency overlap signals in single-channel[5]. FPGA technology integrates the advantages of DSP and ASIC, and it has the characteristics of strong configurability, fast speed, high density and low power consumption. Besides, it is easy to realize thestructures of the parallel and pipeline. The MPSK signal modulator of time and frequency overlap in single-channel based on FPGA can improve the operation performance of the whole device[6].

II. ANALYSIS AND DESIGN OF ALGORITHM

A. The identification algorithm of time and frequency overlap signals in single-channel

Single-channel time and frequency overlapping modulation classification of MPSK double signals is a classification algorithm based on higher-order cyclic-cumulant. The classification characteristics of signal in cyclic-cumulant domain are constructed by using cyclostationary characteristic of signal source. The extraction of classification feature is based on signal four-order cumulant[7]. Then, the single-channel time and frequency overlapping modulation classification of MPSK will be easy. The single-channel time and frequency overlapping modulation classification of MPSK algorithm has better noise resistance ability. And it won't be influenced by the spectral overlap. The recognition processes of single-channel time and frequency overlapping modulation classification of MPSK signals are as follows[8].

Step1: Pretreatment of the input mixed-signal is important. Using the Hilbert-transform transfers the input signal into the corresponding analytic signal. Step2: According to the frequency and symbol rate we can separately estimate signal four-order cumulant and at the baseband of cyclic frequency .Step3:We can calculate the results of four-order cyclic cumulant by using $\beta 1$ and $\beta 2$ at the baseband cyclic frequency. Step4:We extract the classification feature vectors A1 and A2,thenmodulation

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type is recognized by using the minimum error criterion algorithm.

B. Design of signal recognition device

The recognition processes of single-channel time and frequency overlapping modulation classification of MPSK signals are as follows: We can know MPSK signal of four-order cumulanttable from Table1.1.

Table 1.1 Four-order cumulant

TABLE I. FOUR-ORDER CUMULANT

	CA,40	CA,41	CA,42
BPSK	-2E2EJ4Φ	-2E2EJ2Φ	-2E2
QPSK	E2EJ4Φ	0	-E2EJ4Φ
8PSK	0	0	-E2EJ4Φ

We can use the data in the table 1 to construct classification characteristic vectorsA1 and A2classification characteristic vector is F=[A1,A2]. Then, we can get the basic formula of four-order cyclic signal estimation in cumulant cyclic frequency[2].The different orders of MPSK signal eigenvector of classification is different.BPSK modulation signal F=[1,1]; QPSK modulation signal F=[1,0]; 8PSK modulation signal F=[0,0]. Classification guidelines:When T=$\sum_{i=1}^{2}|A'-A_i|$, the 'T' indicates the difference of actual value and theoretical value. Actual signal must calculate with 3 kinds of theoretical signal. When the value of 'T' is the lowest, the result is the actual signal.

C. Serial and parallel conversion

Serial and parallel conversion is one of the most important FPGA design skills. It is a common means of high-speed data stream processing,there are many methods to implement serial and parallel conversion. According to data of the sort and amount,we can choose to use registers, dual-port RAM (DPRAM),single-port RAM (SPRAM), FIFO implementation[9]. It's easy to implement serial and parallel conversion by VHDL. Here are 3 steps. step1: input data Serial number EN(enter number)take the remainder with 2.Based on the results we can draw 2 output 'I' and 'Q'。 step2: IF EN%2=0,the result will output by 'I' . step3: IF EN%2=1, the result will output by 'Q'('%' means take the remainder). Differential encoding is a good way to implement serial asynchronous communication. In this paper , we implement signal serial and parallel conversion by differential encoding .

D. Design of serial and parallel conversion module

The way to implement signal serial and parallel conversion is differential encoding. In other words, except the first element, each element is encoded by itself and its preceding element the deviations.Differential encoding implementations is shown in Fig.1.

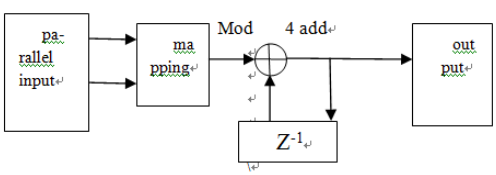

Figure 1. Differential encoding implementations

E. Design of modulator

The modulation system schematic diagram is displayed in Fig.2.

Serial and parallel conversion device convert serial data to parallel data whose rate is reduced to a half. Then, the source signals are coded by differential encoding device. The clock controls carrier waveform. The identification device of time and frequency overlap signals in single-channel can identify the kind of signal. It can identify BPSK, QPSK and 8PSK.

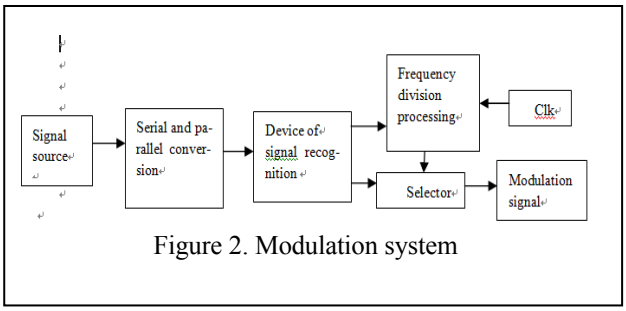

Figure 2. Modulation system

III. TEST AND ANALYSIS OF THE SYSTEM

A. Simulation of signal recognition algorithm

The simulation experiment 1: We can get the recognition performance of MPSK signals in different combinations with same signal power [10].

TABLE II. RECOGNITION PERFORMANCE

MODULATION COMBINATION	-5DB	0DB	5DB	10DB
BPSK&QPSK	0.23	0.39	0.53	0.71
BPSK&8 PSK	0.37	0.77	0.96	0.94
QPSK&8 PSK	0.20	0.30	0.72	0.87

From table 2, In the case of signal-to-noise ratio over 5dB, signal recognition algorithm hasgood classification performance. So it can be used to design the classifier.

In the simulation experiment 2: we test the spectral overlap influence on the performance of signal recognition. Spectrum overlap is defined as the ratio of double signal frequency domain overlapping part and double signal bandwidth. We use the following 3 different signal data of

carrier frequencies and bit widths to test. The first set of data: f1=0.4, T1=25 and f2=0.4, T2=20.Their spectral overlap is greater than 80%. The second set of data: f1=0.44, T1=25 and f2=0.4, T2=20.Their spectral overlap is approximately equal to 50%. The third set of data: f1=0.4, T1=25 and f2=0.48, T2=20. Their spectral overlap is less than 20%. Sampled data of signal is 2000 points.

We can know that spectral overlap has little effect on recognition performance from Fig.3.This algorithm has good recognition stability.

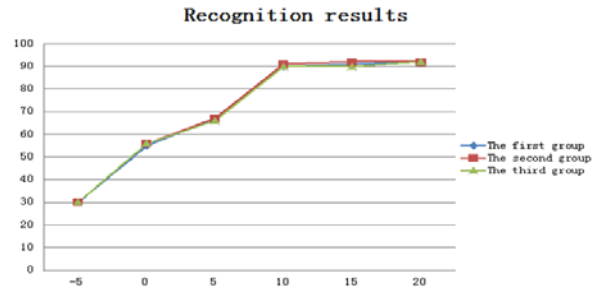

Figure 3. Simulation result

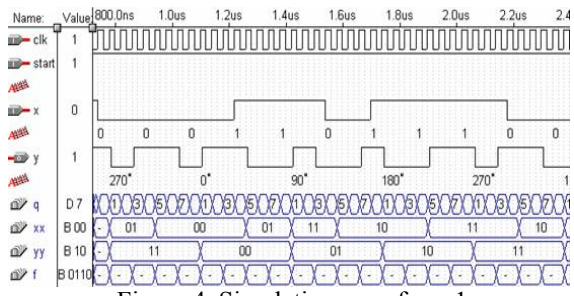

Figure 4. Simulation waveform 1

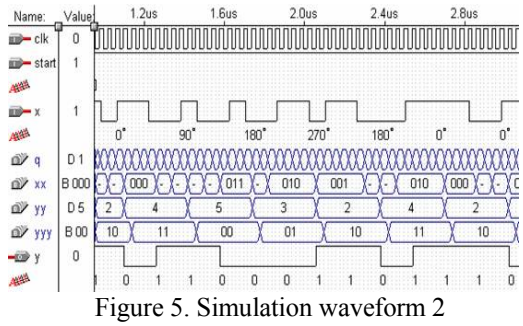

Figure 5. Simulation waveform 2

IV. Simulation and Analysis of MPSK Signal Modulation

This design uses the hardware description language VHDL to program, Quartus II 8.0 to integrate and wire, and ModelSim platform to simulate[11]. The Fig.4 is the simulation of modulation. This modulated waveform is the result when the input signal is QPSK.

The Fig.5 is the demodulation of modulation. This modulated waveform is the result when the input signal is QPSK.

V. Conclusions

This design implements the recognition of modulation types by separating the module. We merge all modules and implement the MPSK signal modulator based on FPGA with the function of signal sort recognition. It can automatically identify the source of the signal and then directly implement the modulation of MPSK signals. The design implements the function of integration, and reduces cost[12,13]. The premise of achieving the identification algorithm of time and frequency overlap signals in single-channel is that we can estimate in advance the carrier and bit rate of dual signal. Therefore, recognition performance is largely influenced by the estimation error of two parameters. The classification result is not too ideal when the signal-to-noise ratio is in the range of -5db and 0db. Those all need to be improved
in future.

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