The Design and Hardware Implementation of OFDM System Receiver Based on FPGA

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Abstract-In recent years, new communication technologies has made rapid development. Orthogo-nal Frequency Division Multiplexing (OFDM) is a core technology in the fourth-generation wireless communication field(4G). The basic principle of OFDM is to split a high-rate data stream into a number of lower. In OFDM system design, a number of parameters are up for consideration, such as the number of subcarriers, guard time, symbol duration, subcarrier spacing, modulation type persubcarrier, and the type of forward error correction coding. The choice of parameters is influenced by system requirements such as available bandwidth, required bit rate, tolerable delay spread, and Doppler values. This paper designs and implements an OFDM receiver system. The system includes interleaving and de-interleaving module, RS encoding and decoding module, QPSK modulation and demodulation module and some system composed of a number of auxiliary modules. This paper analyses and tests efficiency and other factors of the system, and demonstrating the use of FPGA technology enables to receive signal in the OFDM system so well. It has some advantages of occupying less hardware resources, fast running and having good stability.

Key words-OFDM; Wireless communication; FPGA; Receiver; 4G

I. INTRODUCTION

OFDM technology, also called orthogonal frequency division multiplexing, which is the hot technology of thecurrent research. In fact, OFDM is a multicarrier modulation technology. The main idea of the OFDM is to split the data stream to be transmitted into N parallel streams of reduced data rate and to transmit each of them on a separate subcarrier[1,2]. These carriers are made orthogonal by appropriately choosing the frequency spacing between them. Therefore, spect-ral overlapping among subcarriers is allowed. Si-nce the orthogonality will ensure that the receiver can separate the OFDM subcarriers, and a better spectral efficiency can be achieved than by using simple frequency division multiplex[3].

From the basic principle of wireless communication, this paper discusses the key factors that affect the quality of wireless communication. This paper uses the advanced technology of FPGA to achieve a OFDM system. The system includes interleaving and de-interleaving module, RS encoding and decoding module, QPSK modulation and demodulation module and some system composed of a number of auxiliary modules. At last, this system, through the simulation of ModelSim software is analysed in some aspects of performance, such as the efficiency, the expense and the error.

II. IMPLEMENTATION OF OFDM SYSTEM RECEIVER

In the process of the wireless communication, the Doppler frequency shift of channel, multipat-h propagation and fading, noise interference in the channel, directly acting on the receiving part of the system, are important for the design and implementation of a receiver in a communicatio-n system[4]. Because the performance of the receiver determines the communication quality of the whole communication system[5]. So it is necessary to know the theory of receiver and the method of designing receiver. In this chapter, we focus on the design and implementation of the receiver. The steps of system's data receiving follow Fig .1.

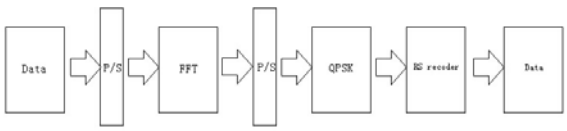

Figure 1. The steps of system's data receiving

After serial to parallel conversion, the signal is passed into the FFT module as shown in figure 1. And then, the signal is output, after parallel to serial conversion and demodulation of the modulation. The decoding function obtains the required data. The process of receiving data and sending data are opposite. We use the clock signal that is inside the system. Each part can be realized by the

technology of FPGA. The structure of the system designs as below in Fig . 2.

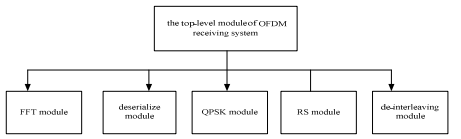

Figure 2. The structure of the OFDM system

The whole system includes the FFT module, interleaving and de-interleaving module, RS encoding and decoding module, QPSK modulation and demodulation module and some system composed of a number of auxiliary modules. Next, we will design and implement the relevant modules of the system.

A. Implementation of interleaving and de-interleaving module

For the OFDM system, the interleaving and de-interleaving technology is the important part of the whole communication system[6]. The main function of the interleaver is to disrupt the order of the input data and to change the original structure of the data. For the sequence of data, the correlation is reduced, but the content of the input data is not changed[7].This can effectively resist the harm caused by the sudden errors in the channel. The process of de-interleaving can be used the opposite method to recover the original data. The symbol file of the interleaver is generated as follows in Fig .3.

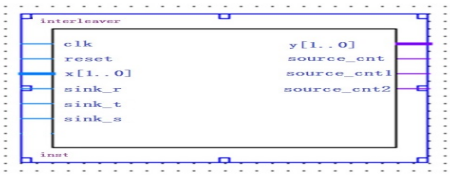

Figure 3. The symbol file of the interleaver

B. Implementation of RS encoding and decoding module

The Reed-Solomon RS code named as Reed and Reed-Solomon is a typical BCH code. It has a very strong ability of error correcting[8].It is widely used to code channel and store data in the field of wireless communication. In the OFDM system, it is not only to guarantee the higher abilities of correcting error, but also has certain request of the data transmission rate. Not only we need a high coding efficiency, also consider the coding algorithm and the structure of circuit. So the selection of RS code is more appropriate. For the part of multiplier , we can use the method that is look-up table to reduce the occupied resources. We can design the multiplier as a fixed form. It also satisfies the characteristics of the coefficients in the Polynomial. Its principle is easy to understand and implement. The symbol file of the RS decoder is generated as follows in Fig .4.

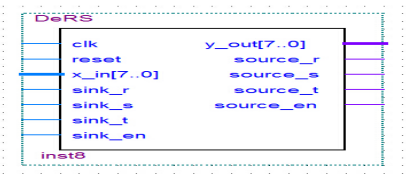

Figure 4. The symbol file of the RS decoder

C. Implementation of QPSK modulation and demodulation module

The quadrature phase shift keying (QPSK) is a kind of digital modulation method. QPSK modulation uses the method that is diffusing energy as random, and its goal is to handle data flow[9].

QPSK also can deal with the RS coding, conv-olutional interleaver, convolution coding, etc. It ensures the transmission performance of the data. QPSK modulation has a strong ability that is anti-interference .QPSK modulation has some advantages that have a strong anti-interference, a good spectrum utilization and a good compatibility[10].The symbol file of the QPSK modulation is generated as follows in Fig .5.

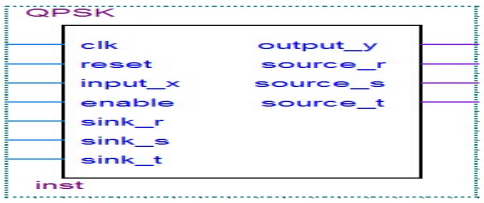

Figure 5. The symbol file of the QPSK modulation

D. Implementation of deserialize and FFT module

1) Implementation of deserialize

In the wireless communication system, the serial to parallel and parallel to serial are very common and important link. t is a method of dealing with the signal. It can transform a group of signal into a set of parallel signal. At the same time, it does not change the information of the signal carried. The symbol file of the serial to parallel is generated as follows in Fig .6.

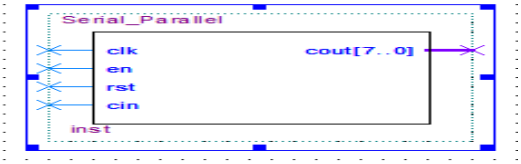

Figure 6. The symbol file of the serial to parallel

2) Implementation of FFT module

FPGA has rich applications, which contain the IP core of Altera. These IP cores have good compatibility.

III. The results and analysis

A. RS decoding module and FFT module

For the RS decoding module, the simulation result is generated as below in Fig .7.

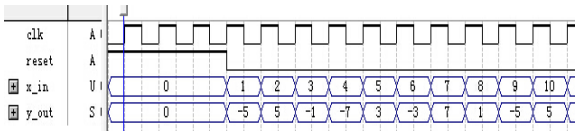

Figure 7. RS decoding module simulation

The data from one to thirty six is inputting, and the value of every 6 number takes for the output data. That is the matrix inputting by row and outputting by column. The logical function is consistent with the expected design. Also, this shows the correctness of the hardware implementation. Due to the setting is eight bit data, so the signal transferring in module is eight bit.

For the FFT module, it can be applied to the system.

B. QPSK Modem module

Fig .8 is the simulation result of the QPSK module. The symbol of CLK is the system clock and the symbol of reset is enable signal. The symbol of X is the input data signal and the symbol of Y is the output results.

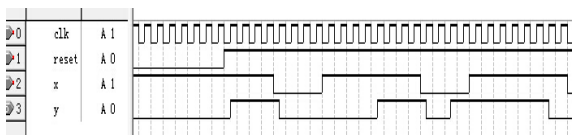

Figure 8. QPSK modulation simulation

C. Serial-to-parallel conversion module

In the process of the Serial-to-parallel conversion, the newly input data become the lowest bit of the original data and give up the highest bit of the original data[10]. First, eight bits data stored in a register and then, the data shifts left outputting one by one. The simulation result is consistent with the expected design. This illustrates FPGA can better realize Serial-to-para-llel conversion. The simulation result is generated as show in Fig .9.

D. System verification

The integer simulation is generated as below in Fig .10.At 170ns, the signal corresponds the value that is 00101 in the register. The number of matching interval is 3, which the system receives. The output results are basic

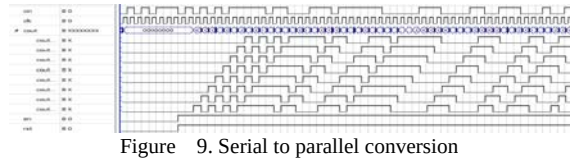
Figure 9. Serial to parallel conversion

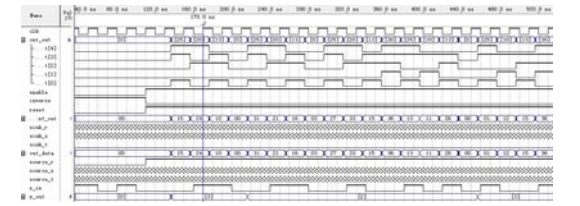
Figure 10. The system simulation implementation

the same as the input values. The logical function of the receiver is consistent with the expected design. This fully demonstrates the correctness of the design.

IV. CONCLUSIONS

This paper is further analysis the possible of the hardware implementation of OFDM systems technology. On this basis, it designs and implements an OFDM receiver system. This system provides further reference to research OFDM system. Also it provides valuable experience to complete the simulation using the hardware communications. This design still exists deficiencies. The ideas of existing module design are unitary. The design of the module is not very complicated. The problem of complex system can not be well solved. This can be another innovation point in the future study of OFDM.

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