# Design and Implementation of the Scan Digital Display Based on FPGA

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**Abstract—The scan digital display has the function of receiving and processing digital signals. As an advanced display type, the digital display presents a trend of accelerating development. Because of shortage of the long development cycle and high price of the traditional display design, this paper designs a scan display with six-bit Nixie tubes to achieve dynamic refresh display based on FPGA. This design adopts EDA technology, using VHDL as the hardware description language and Quartus II as the development platform to construct the scan digital display, which consists of the DATA module, multi-channel data selection module and BCD decoding module. Finally, the correctness and effectiveness of the digital display is validated by the compilation and simulation of the program downloaded from the programmable logic devices. This scan digital display has the characteristics of high speed, low power consumption and low cost which can be widely used in the market.**

***Keywords-FPGA; EDA technology; VHDL; scan digital display.***

## I. INTRODUCTION

The digital display is a display with the function of receiving and processing digital signals, which is widely used in various fields and brings much convenience to people's life[1].

The system of scan digital display discards the old work way of putting monitoring and calculation together and the way of setting status. At present, the design platform of the scan digital display is mainly conducted on single chip, while in this paper, the design is based on FPGA. FPGA is referred to the field programmable gate array. The design of FPGA device is flexible and convenient, which can be programmed more than once with the characteristics of high speed, low power consumption and low cost. Using FPGA to develop the digital system can significantly shorten the design time, reduce the number of peripheral circuit and development costs, and improve the reliability of the system.Therefore, realizing the digital scan display has an important realistic significance.

This paper designs a scan display with six-bit Nixie tubes to achieve the dynamic refresh display based on FPGA. It adopts EDA technology, using VHDL as a hardware description language and Quartus II as the development platform to construct the scan digital display[2,3].

Firstly, the digital scan display uses FPGA chips to input clock and divide the counter to 1Hz in DATA module. Secondly, the design processes the data through the multi-channel data selection module.

And then the BCD decoding module decodes the processed data to achieve the dynamic refresh display[4].

## II. DESIGN OF SCAN DIGITAL DISPLAY BASED ON FPGA

### *A. Algorithm design of scan digital display*

Digital display has a wide using spectrum in the agricultural production, aviation, transportation, health care, instrumentation and technology industry with the integration of civil and military. There is no doubt that the digital scan is an indispensable part of the modern society[5].

There are two kinds of ways of digital display, static display and dynamic display.

When it works in static way, bit lines of the digital tube is connected with the power. Each digital tube is in a power-on state, and the signals waiting for displaying transmit to the display circuit after decoding. Then each digital tube receives and display their signals respectively in the same time. That is to say, in the static operation mode, the bit lines of the digital tube in the display circuit is conducted in the same time, but the digital control of each line is independent.

When it works in dynamic way, the bit lines of digital tube is conducted according to the set order under the control of the scanning control circuit.The digital tube is individually connected to the power supply, and the control line of digital tube connects with the decoding circuit in parallel. Then the scanning control circuit transmit the signals to the digital tube one by one according to the set order, and the digital tube also shows the characters in the same way. That is to say, in the dynamic mode, the digital tube doesn’t be conducted in the same time and it is displayed according to set the order[6].

The dynamic scan display of Nixie tube, namely sending the font code and the corresponding bit selection to Nixie tubes in turn, gating to the six-bit Nixie tube in cycle. The aim is to make people believe that each tube is

 

displaying through the effect of human eye's persistence of vision and the twilight of luminous Nixie tube, in fact, which displays bit by bit in turn[7].

We designed a six-bit number, whose circulation moving is achieved in the way of moving from left to right until the maximum bit removes the rightmost digital block. The lowest bit moves into from the leftmost digital block[8]. We realize the control of Nixie tube by decoding, and the flow chart of the algorithm designed is shown in Fig. 1.

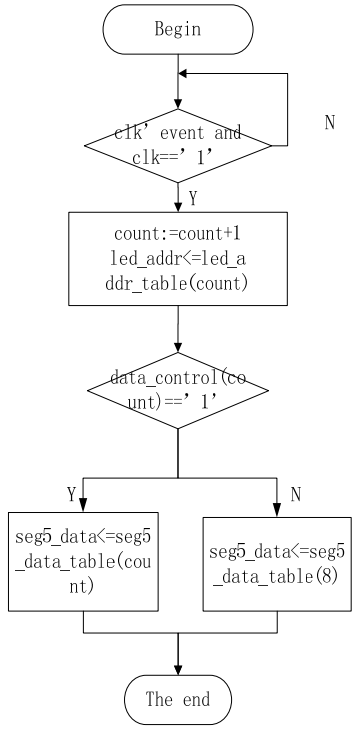


Figure 1. The flow chart of the algorithm design

## B. *Overall design and function analysis of modules*

In this paper, we design a scan display which enables a six-bit nixie tubes achieve dynamic refresh display. This design adopts EDA technology, using VHDL as the hardware description language and Quartus II as the development platform to construct the scan digital display. The overall design of the system can be divided into three modules, namely DATA module, MULX module, and BCD_LED module, and each module has its own principles and functions.

These modules are shown in Fig .2, Fig .3, and Fig .4.

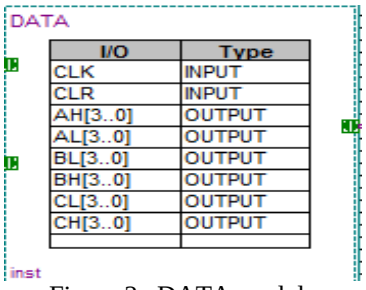


Figure 2. DATA module

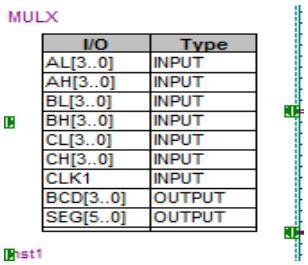


Figure 3. MULX module

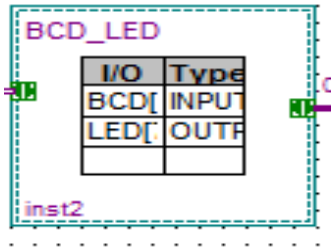


Figure 4. BCD_LED module

DATA module: Its main function is to process binary numbers, and converse various binary numbers into senary scales, and assigns them to corresponding pins.

MULX Module: This module is a data selection multiplexer, which is designed for achieving the conversion of logic functionality of data processed by DATA module.

BCD_LED module: The module is designed for decoding the data transferred by the logic circuits, and then outputs the logic results.

In this design, we established a senary counter firstly, where each 4 bits binary number represents a senary scale, which is defined as DATA module, and this module converses the binary numbers inputted into senary scale and counts.

Next, we designed a data selection multiplexer, which is defined as MULX modules, and this module will process various cases of data and data itself processed by DATA module.

And then it transfers them to the BCD decoder, which is defined as BCD_LED module, this module will decode the data transmitted by the logic circuits, and output it after completing the pin assignments,

Finally, we can get the final logic results. The top-level design schematic of the overall system design is shown in Fig .5.

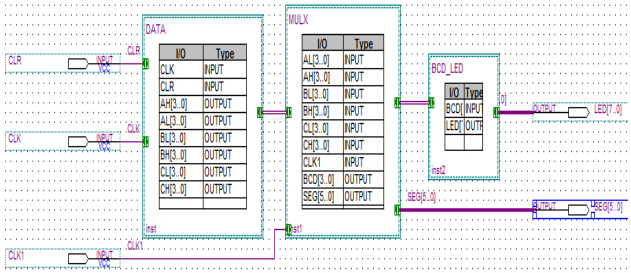


Figure 5. The top-level design schematic of scan digital display

## III. Simulation of Scan Digital Display and Analysis of Simulation Results

The simulation waveform window of the half-adder we get after the successful function simulation is shown in Fig .6.

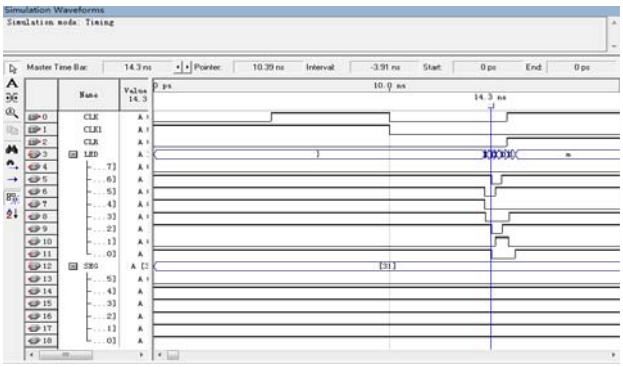

Figure 6. The simulation waveform window of the half-adder

After the program starting, we first determine whether the data is true inputted from clk, and the true value is 1. If it is true, we will count for each true value and expressed by the count in Fig .5, and then we need determine whether the address assigned when the data inputs is larger than the address assignment designed by system of scan digital display, if yes, the input will be invalid, otherwise, the input data will be inputted and recorded into tables. Then system will converse these binary datas inputted into senary scale data and store the data successfully converted in the table(count), and then process the output display, completing the overall design of scan display[9]. Meanwhile, the data unsuccessfully converted will be stored in the table(8), and carry out the error handling.

The timing simulation results and the function simulation results obtained after completing the overall design are shown in Fig .7 and Fig .8 respectively.

Where, we can prove whether the logic function of our design is correct by analyzing the waveform shown in Fig . 7. If it is correct, we will assign the corresponding pins and validate after configuring the results to chips, otherwise, we have to return to the previous step to modify. The logic function of our design is correct after verifying.

From the waveform of the lower part of Fig .8, we can see that the wave form is a ladder-type, because we designed to make a six-bit number moving in the way of from left to right, until the maximum bit removed the rightmost digital block, and then the lowest bit moves into from the leftmost digital block to achieve the data's circulation moving. And can be seen from the Fig .8, these waveforms consist of a waveform diagram in an infinite loop, so the logic function of the circuit we designed can meet the design requirements.

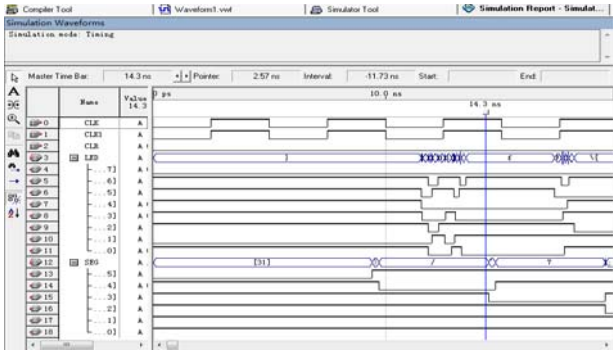

Figure 7. The overall timing simulation waveform

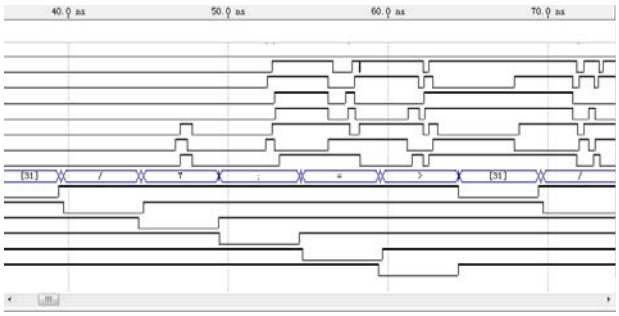

Figure 8. The overall function simulation waveform

## IV. Summary

In this paper, we designed a scan display which enables a six-bit Nixie tubes achieve dynamic refresh display based on FPGA. Using EDA technology, VHDL hardware description language, and Quartus II development platform, we built the scan digital display with the DATA module, MULX module, and BCD_LED module, and realized its dynamic scanning display. We verified the correctness and validity of the digital display by compiling and simulating the programming. The design of FPGA device is flexible and convenient, which can be programmed more than once with the characteristics of high speed, low power consumption and low cost.

The scan digital display designed based on FPGA can significantly reduce the design time and development costs[10]. We consider that putting this design into production and to the market in future.

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