The Optimization Scheme Of The Leakage Current Reduction Technique For SRAM Design

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Abstract—An optimization scheme of the leakage current reduction (LCR) for SRAM design has been proposed in this letter. By choosing the enabling signals for the LCR circuits intentionally, it can be deduced theoretically that there exists an optimal design option for the LCR technique application under the premise of SRAM performance re-quirement. Assuming that the reliably of SA sense requires 100mV differential voltage of bitlines, and the number of bitcells attached to one bitline is 2048, the simulate results shows that the discharging rate under the value of 256 of k is the fastest which is conform to the theoretical calculation, which means the most significant reduction of leakage current.

Keywords-component; SRAM; Leakage current reduction (LCR); Optimization

I. INTRODUCTION

As the semiconductor technology progresses, the leakage current demonstrates an ever increasing trend [1-2], which would incur many challenges for SRAM design. The large leakage current existing in the circuit may cause the SRAM read performance to be degraded or even malfunctioning [2-6]. As a result, the leakage current reduction (LCR) technique is always employed to tackle this issue by reducing the leakage current directly.

The major LCR techniques employed [7-10] are shown in Fig. 1, which consist of sleep transistor and virtual ground technique, as Fig. 1a shown; reverse body bias technique, as Fig. 1b shown; stacked transistors technique, as Fig. 1c shown. All these techniques can be applied individually or in tandem. Besides, the symbol of Fig. 1d represents the LCR circuit employed to apply the LCR technique conditionally according to the enabling signal EN, which means that when EN=0, the leakage current reduction circuit is effective, otherwise it brings the circuit to normal as if no leakage current reduction techniques have been applied.

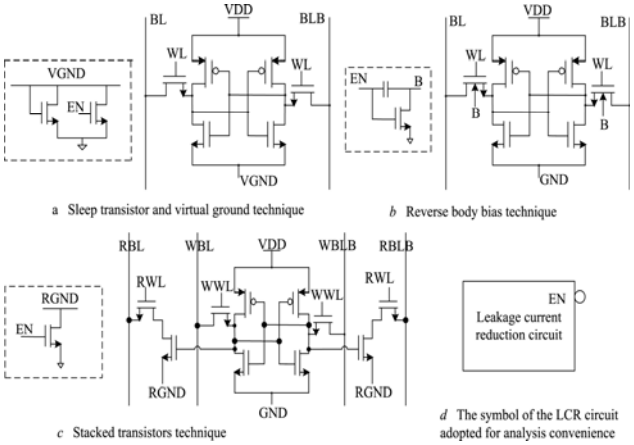

Figure 1. Major LCR techniques for SRAM design.

The symbol of the LCR circuit in Fig. 1 is adopted in this letter to facilitate the analysis and optimize the SRAM design. The optimization scheme starts from the selection of the enabling signals for the LCR circuits. Assuming that the whole decoder of the SRAM is a m-to-n decoder and the decoder adopts a two-level architecture, which contains two pre-decoders and one post-decoder, as shown in Fig. 2a. P_1~P_k is decoded by the pre-decoder (1) and Q_1 ~$Q_{n/k}$ is decoded by the pre-decoder (2). The combination of P_1~P_k and Q_1~$Q_{n/k}$ together will decode the whole n word-lines. Specifically, this decoder structure divides the SRAM bit-cell bank into n/k parts and each part contains k bit-cells so that the signals Q_1~$Q_{n/k}$ can be employed to provide the enabling signals for the LCR circuit. The reason is that if one of the n/k signals is "1", then there would be one bit-cell in this part to be accessed and the other bit-cells of the n/k-1 parts will not be accessed. Therefore, the n/k-1 parts of one column bit-cells can be applied with the technique of LCR and leaving the only part selected to be intact. As a result, the whole schematic for the optimization design can be constructed in Fig. 2 as follows.

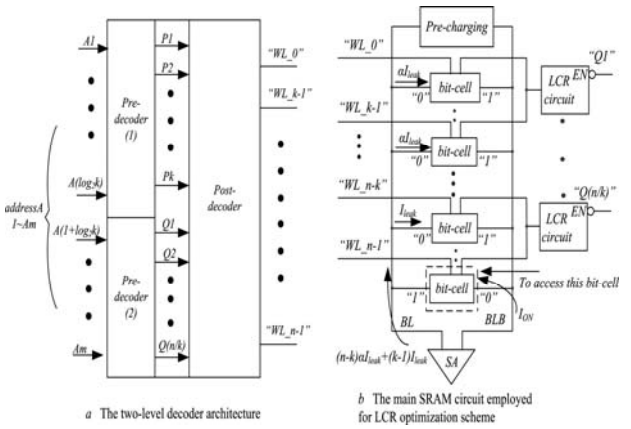

Figure 2. the whole schematic circuit for optimization design.

As shown in Fig. 2b, the worst case situation when the accessed cell being read contains a "1" and all the others in the same column contain a "0" is considered and the parameter α in the plot represents the efficiency of the LCR technique, which means that the leakage current would be reduced to α times of the previous leakage value if the LCR circuit is valid. As a result, the current distribution can be deduced if the last bitcell is accessed:

$$I_{BLB} = I_{ON}$$

$$\begin{aligned} I_{BL} &= (n-k)\alpha\ I_{leak} + (k-1)\ I_{leak} \\ &= \alpha n\ I_{leak} + k(1-\alpha) - 1)\ I_{leak} \end{aligned}$$

Where I_{leak} is the single leakage current flowing into the bit-cell without the usage of the LCR technique. Therefore, it is shown from equation (2) that the current on the BL bit-line will be increased with the growing of k so that the ratio of the discharging current of the two bit-lines will be decreased which will lead to the degradation of performance. Then the question raises that what specific value of k should be chosen under the premise of performance requirement. The choice of k is elaborated as follows.

II. Optimization Design for LCR Technique

The optimization design for LCR technique begins by examining whether the shortest delay that can be achieved through LCR technique is smaller than the delay that satisfies the performance requirement of the whole SRAM. As can be deduced previously, the shortest delay can be obtained by making the enabling signals to be the word-lines, respectively so that the leakage current can be reduced to a maximum extent. Supposing the shortest delay is smaller than the required performance and the corresponding optimization design is elaborated as follows.

Assuming that the ratio of the discharging current of the two bit-lines without the usage of the LCR technique in the worst case is $=I_{BLB}/I_{BL}$ and the ratio that satisfies the performance requirement is annotated to be $\sigma = I'_{BLB} / I'_{BL}$, where the prime in the expression demonstrates the corresponding value with the usage of the LCR technique in the worst case, then the expression of σ' can be deduced as follows:

$$\begin{aligned} \frac{\sigma'}{\sigma} &= \frac{I'_{BLB}/I'_{BL}}{I_{BLB}/I_{BL}} = \frac{I_{on}/I'_{BL}}{I_{on}/I_{BL}} = \frac{I_{BL}}{I'_{BL}} \\ &= \frac{(n-1)/I_{leak}}{(k-1)/I_{leak} + (n-k)\alpha/I_{leak}} \\ &= \frac{(n-1)}{(1-\alpha)k - 1 + \alpha n} \end{aligned} \tag{3}$$

As a result, the value of k can be deduced according to equation (4) as follows:

$$k = \frac{\alpha(n-1)/\sigma' + 1 - \alpha n}{1-\alpha} \tag{4}$$

Because k is decoded from the pre-decoder (1) addressed by A_1~A_{log2k}, the value of k should be the exponential value of 2. Besides, the smaller the value of k is, the larger the corresponding current ratio is, which is more beneficial for the performance improvement. As a result, the optimal value of k can be deduced as a common equation as follows:

$$k = 2^{\left\lfloor \log_2\left(\frac{\sigma(n-1)/\sigma^{prime} + 1 - \alpha n}{1-\alpha}\right)\right\rfloor} \tag{5}$$

But the expression in equation (5) is over-abstract for it does not unveil the specific relationship between k and the other important parameters of SRAM such as the time satisfied with the performance requirement and so on. Consequently, it is necessary to deduce further on the basis of equation (5).

Supposing that the time satisfied with the performance requirement is T_{access}, and then the maximal leakage tolerable in the worst case can be calculated as follows:

$$T_{access} = \frac{C_{BL}\Delta V_{BL}}{I_{on} - I_{leak\_tolerable}} \tag{6}$$

Where C_{BL} represents the parasitic capacitor of bitline and ΔV_{BL} represents the minimum differential bitline voltage needed for SA detection. Therefore, the maximal leakage tolerable in the worst case can be deduced to be:

$$I_{leak\_tolerable} = I_{on} - \frac{C_{BL}\Delta V_{BL}}{T_{access}} \tag{7}$$

Therefore, the ratio that satisfies the performance requirement can now be demonstrated as follows:

$$\begin{aligned} \sigma' &= \frac{I_{on}}{I_{leak\_tolerable}} \\ &= I_{on} / \left(I_{on} - \frac{C_{BL}\Delta V_{BL}}{T_{access}} \right) \\ &= \frac{I_{on} T_{access}}{I_{on} T_{access} - C_{BL}\Delta V_{BL}} \end{aligned} \tag{8}$$

Then the expression of σ' / σ can be deduced as follows:

$$\frac{\sigma'}{\sigma} = \frac{I_{on}T_{access}}{I_{on}T_{access} - C_{BL}\Delta V_{BL}} \frac{(n-1)I_{leak}}{I_{on}} = \frac{(n-1)I_{leak}T_{access}}{I_{on}T_{access} - C_{BL}\Delta V_{BL}} \quad (9)$$

Putting the expression of (9) into (5) can obtain the new expression of k as follows:

$$k = 2^{\left\lfloor \log_2\left(\frac{\frac{I_{on}T_{access} - C_{BL}\Delta V_{BL}}{I_{leak}T_{access}} + 1 - \alpha n}{1-\alpha}\right) \right\rfloor} \quad (10)$$

The value of k attained from equation (10) demonstrates that there exists an optimal value of k theoretically to optimize the LCR design under the premise of SRAM performance requirement.

III. THE SIMULATION RESULTS

In order to verify the effectiveness of the proposed leakage current reduction technique, the 2048 bitcells have been attached to one bitline for the simulation. Considering the worst case where one bitcell stores "0" while the others store "1" on the same column and the bitcell storing "0" is accessed. By proper sizing of the pass transistor and the leakage current reduction circuit, the optimized value of k is calculated to be 256 according to equation (10) for developing 100mV differential voltage. The other situations under different values of k and the situation without using the proposed technique are also simulated for comparison. The corresponding simulation results of differential bitline voltage are shown in Fig. 3.

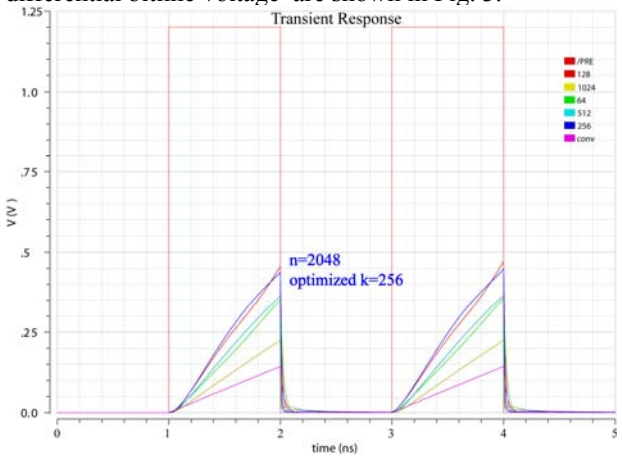

Figure 3. The simulation waveforms under different values of k.

Fig. 3 shows the discharging rate under the value of 256 of k is the fastest which is conform to the theoretical calculation when 2048 bitcells are attached to one bitline. It means the most significant reduction of leakage current occur in the value of 256 of k.

In order to verify the proposed technique further, the quantitative analysis is also taken where 2048 bitcells are attached to one bitline. Assuming that the reliably of SA sense requires 100mV differential voltage of bitlines, and then the delays needed to develop this differential bitline voltage under various values of k and process corners are simulated, respectively, as shown in Fig. 4 as follows. The traditional operation without using the proposed technique corresponds to the situation where k equals to 2048.

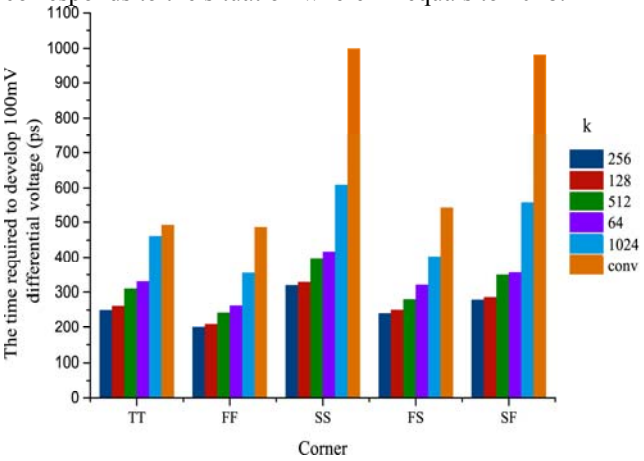

Figure 4. The time required to develop 100mV differential voltage.

As shown in Fig. 4, the delays required to develop 100mV differential bitline voltage under various k are all shorter than the traditional situation under the same process corner. Specifically, under the optimal value of k, the delay reduction can be achieved to the maximum extent under the same process corner. For example, the delay under the optimal situation is 250ps while it is 492ps for the traditional situation under TT process corner, which means that the delay can be reduced to almost 50.8%.

IV. CONCLUSIONS

An optimization scheme has been proposed in this paper for the leakage current reduction technique of SRAM design. The result demonstrates that there exists a theoretical optimal design option of the LCR technique under the premise of SRAM performance requirement and the corresponding simulation results verify the theoretical derivation experimentally.

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