Analysis of Embedded ARM System Design and Application

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Abstract: Based on the single camera 3D refactoring system of ARM+FPGA, this paper designed dicaryon hardware architecture, which takes ARM processor as logic control center and FPGA as co-processor, to complete the design of device driver and partial software. This paper also utilized FPGA to complete the key technical studies of image capture and calculation, 3D image refactor as well as others, besides, it fully utilized C2H and user-defined element, defined instruction and other technology to improve the calculation capability of the system; moreover, it utilized ARM processor specially for 3D image processing engine, GPMC controller, and sophisticated multimedia and network administration function to complete the design of the main control unit.

Introduction

With the increasing development of the computer technology and the occurrence of ARM technology and embedded system, the application field of embedded system is continuously developing, which involves the fields including industrial control, consumer electronics, network communications, scientific research, military and national defense, medical treatment and public health, aerospace etc[1,2,3]. This paper used the way by combining theory with practice, designing and debugging of ARM system to further grasp the design and development of the embedded system.

Based on the single camera 3D refactoring system of ARM+FPGA, this paper designed dicaryon hardware architecture, which takes ARM processor as logic control center and FPGA as co-processor, to complete the design of device driver and partial software. This paper also utilized FPGA to complete the key technical studies of image capture and calculation, 3D image refactor as well as others, besides, it fully utilized C2H and user-defined element, defined instruction and other technology to improve the calculation capability of the system; moreover, it utilized ARM processor specially for 3D image processing engine, GPMC controller, and sophisticated multimedia and network administration function to complete the design of the main control unit.

Overall Architecture Design of the System

When ARM port sent the instruction to FPGA from IIC interface, FPGA will control infrared emitter array to send modulation light to the detected target and control counter register starting count. The camera will detect the infrared ray returning from the detected target to accumulate on the pixel points of the CMOS structure. When the FPGA count reached the set value, the controlling camera will output the image signal.

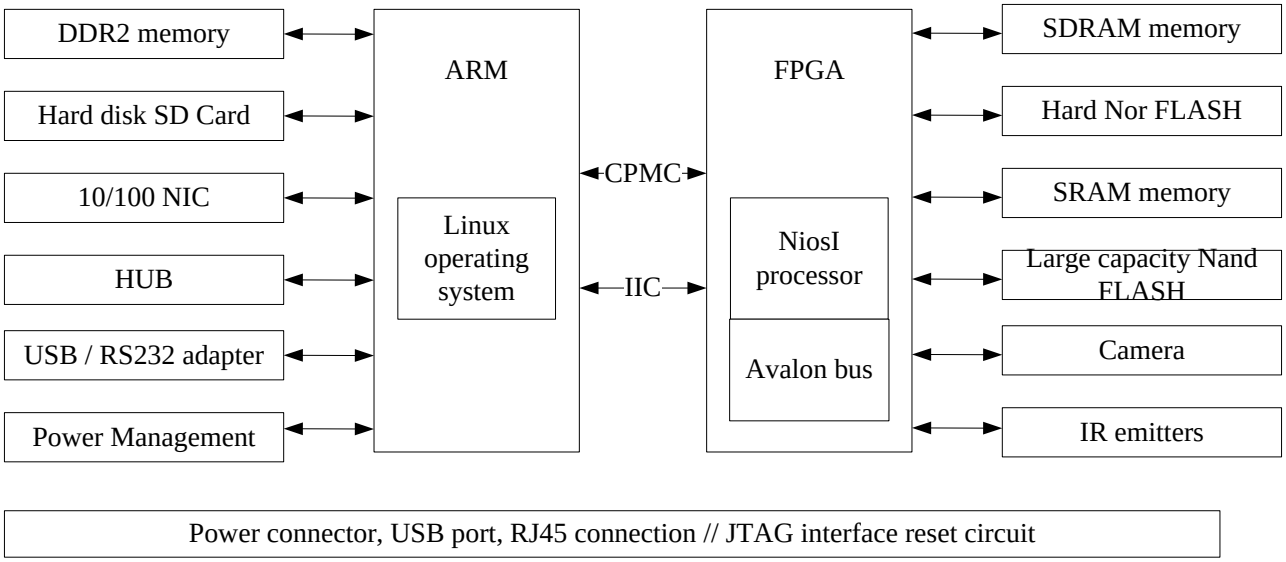

Figure 1 Functional Block Diagram of the System Hardware

As shown in figure 1, FPGA will analyze the phase difference between the infrared reference pulse and the image pulse received by CMOS camera, and invoke FFT to calculate image data to get the 3D data information of the detected target in the end, and store such information in the SRAM of the displayed storage. At this time, ARM will get the feedback signal from IIC by FPGA completing the treatment of one frame image, namely read the 3D image data of SRAM in FPGA system from GPMC interface. After ARM getting data, it will invoke the 3D treatment engine inside ARM to conduct 3D process for the data, and generate the variable views of 3D image and display the image. User can drag, magnify, turn over and do other operations to the 3D image by resistance-type touch screen locating in the LCD screen. In the network safety, network monitoring and other applicaiton fields, this system can serve as embedded WEB server, so user can monitor and control 3D image modelling system by brower at the internet far-end. The system is based on ARM and FPGA to design, through ARM and FPGA to communicate, so as to realize FPGA treated numeral image data transmissing to ARM, and ARM will finish image's storage, playback and other man-machine interaction. See overall system block diagram in figure 2.

This system takes FPGA device as the core. Multicolor CCD camera image will output standard systematical analog video signals, and convert analog video to digital video by video decoding chip to decode. Then FPGA will identify the effective video image data of the digital video flowing to complete image treatment according to the requirement. ARM embedded system will recieve the output instruction of the output device, response the instruction, transmit the instruction to FPGA treatment module to control image treatment. Storage of the treated image is video buffer, the interface logic insisde FPGA will read out video data from video buffer, and input to ARM embedded system through the communication wires between ARM and FPGA, so as to realize image storage, playback and other actions in ARM system.

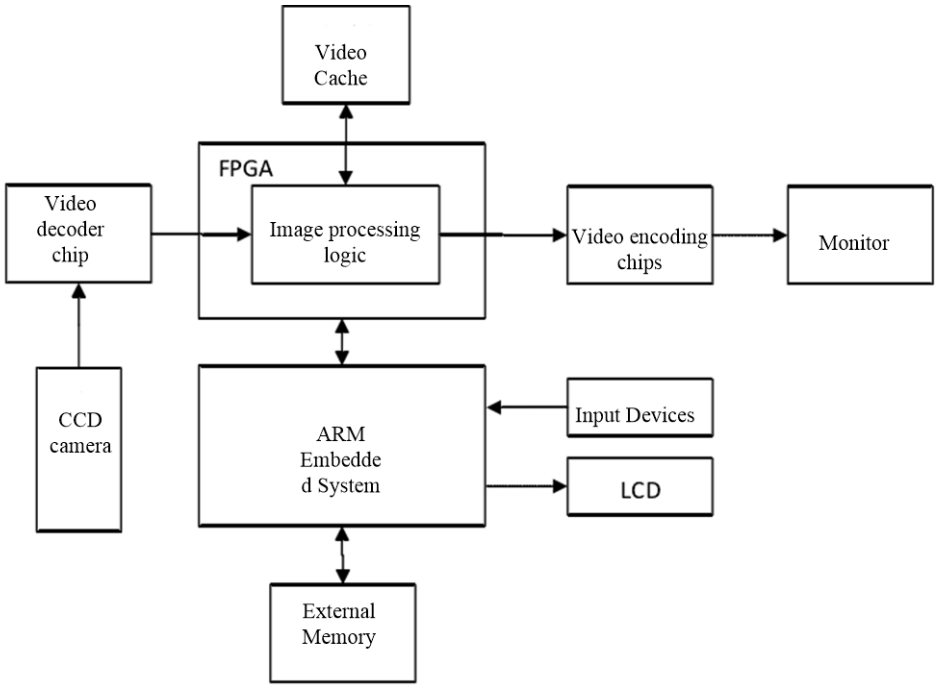

Figure 2 Block Diagram of the System

Hardware design of embedded ARM system

Beaglebone can be used in robort design, motor control, overall model design of automobile CAN, 3D printer design, data backup project design[5,6], SDR(Software DefinedRadio) base station design, USB data collecting board design and other occassions[7,8]. See block diagram of the development board in figure 3. Beaglebone uses a piece of storage with type DDR2 of MT47H128M16RT-25E, as shown in figure 4. There is another piece of EEPROM storage on Beaglebone as the information storage of the development board. Such information includes the name of the development board, series number and version number. The remaining space can be used as the the user-defined space of the program.

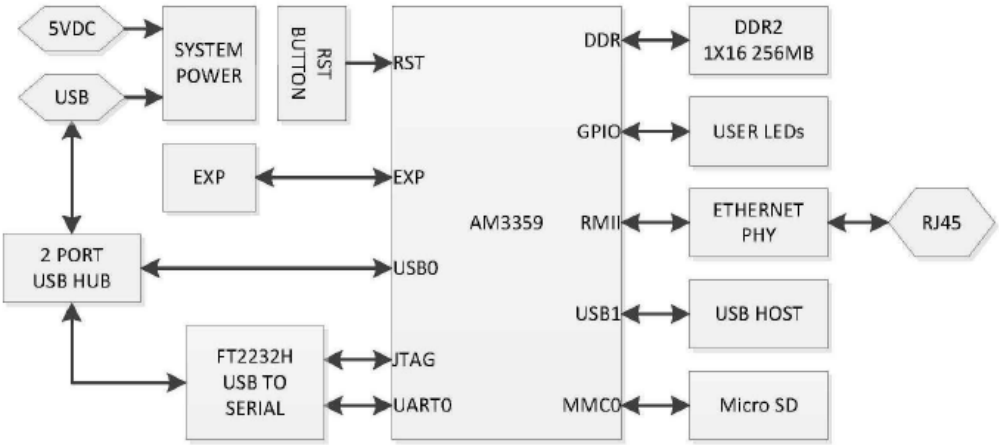

Figure 3 System Block Diagram of the Beaglebone Development Board

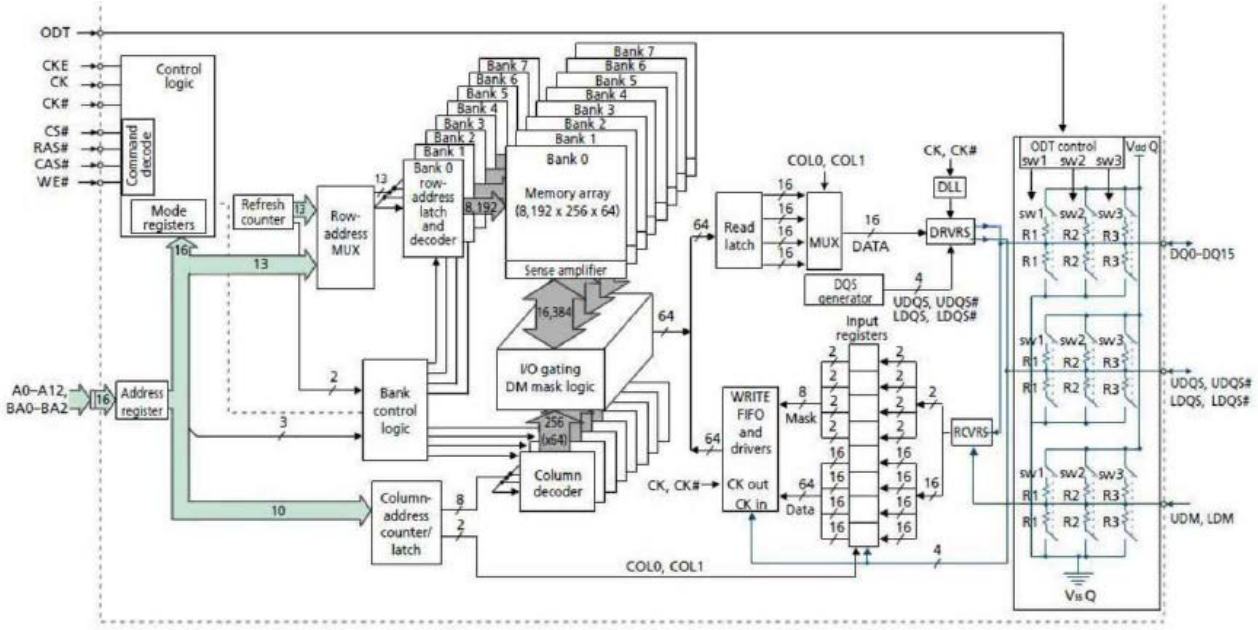

Figure 4 MT47H128M16RT-25E Functional Block Diagram

According to the overall system design, it is needed to use LCD to display 3D model, however, GPMC is the interface of high speed communication between ARM and FPGA. So, this determined LCD cannot be set as RGB888 mode, and GPMC cannot be set as data/address non-reuse mode. Therefore, set LCD as RGB565 mode, and set GPMC as data/addressreuse mode, through which the elevatus LCD data pin can be set as the pin of GPMC, then LCD and GPMC can run parallel without conflict. See the connection between LCD andARM in figure 5.

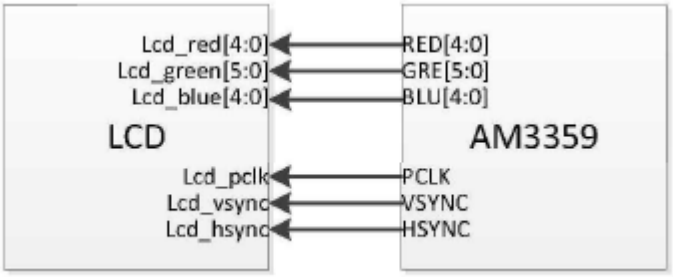

Figure 5 Connection Sketch Map between AM3359 and LCD

In order to meet the timeliness and specificity designing requirement [7], this paper uses FPGA as the 3D scan of the system and controlling core of the 3D printing part. This paper takes FPGA field-programmable gate array as hardware carrier, on which SOC software treatment system and peripheral drive control module are established, so as to realize the followings, such as digital phase-locked loop(PLL), fast fourier transform (FFT), counter, decoder, state machine, general internal storage controller (GPMC) interface and other digital logic, to further realize the main system peripheral design including the controller design of 3D scanner and infrared ray transmitting device. See system block diagram of FPGA in figure 6.

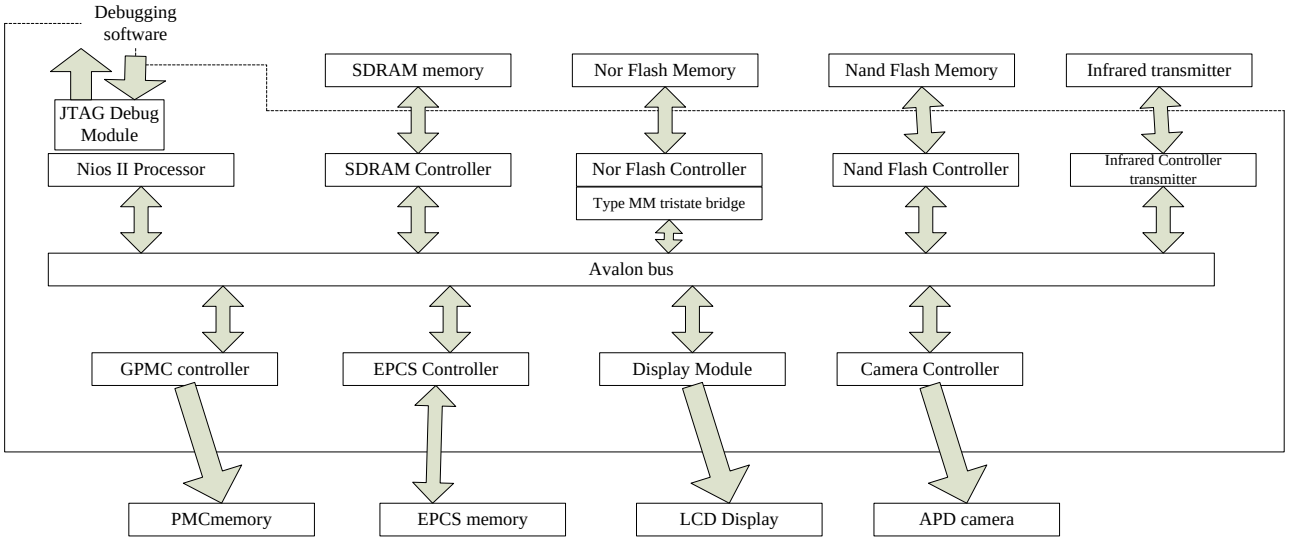

Figure 6 FPGA Block Diagram with Minimum System

ARM and FPGA communication

In this design, directly connect FPGA to the system bus of the ARM system to realize both communications. As both are 3.3V standard, so directly connect signals and connect the areas of both locations. For ARM device, FPGA can be treated as the storage connected on system bus. And ARM can directly visit FPGA by storage visiting instruction. FPGA will connect bank2 storage space of the ARM, ARM can directly visit FPGA by storage visiting instruction, then read the freezing image data. As the clock of FPGA system and ARM system is out of sync, so use an asynchronization FIFO as the data interface between ARM and FPGA. The realization of the communication interface between FPGA and ARM is mainly completed by storage control logic module. See the internal function realization block diagram of the storage controlling logic module in figure 6.

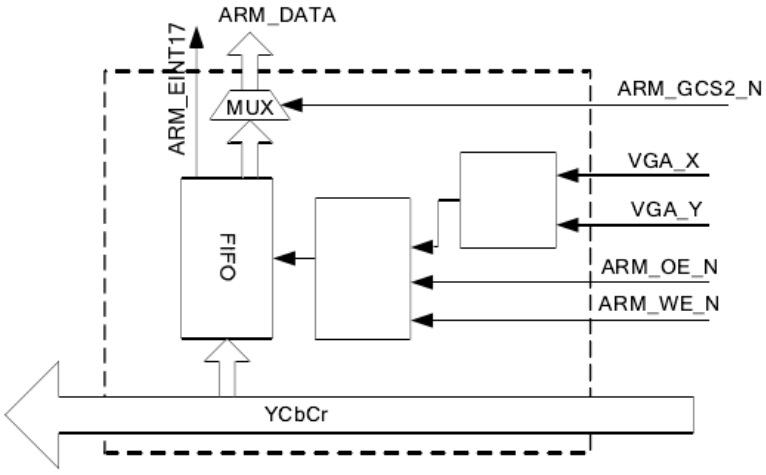

Figure 6 Storage Controlling Logic Module

In order to prevent FIFO output data contaminating the ARM system bus wire, use ARM storage bank2 to select signal GCS2 to control FIFO data outputting to bus wire. When bank2 is selected by ARM, namely ARM is reading FPGA, then output FIFO data to bus wire. Before ARM system start out, GCS2 signal is low level, if GCS2 signal is treated as gating signal of bus wire, it will influence ARM normal operation. Therefore, before image being freezed, it will still keep ARM system data bus wire staying at high resistance status after FPGA reset.

Image FFT design

This paper will use the ranging principle between continous waves based on image FFT conversion to realize the 3D refactor of target object. When FPGA send modulating pulse to infrared transmitter, tranmitter will start transmitting infrared ray. The ray reflected from the measured target will return to camera by the form of analog signal, and project to CMOS array through camera lens focus. The camera will sampling, quantify and coding the simulated image signal to form digital image signal in the end. FPGA will control this image digital signal flowing and store in SRAM video memory. For the time being, image signal due to doppler effect will generate the shift of frequency phase, therefore, there is a phase difference between the signal collected by the camera and reference signal. FPGA will conduct fourier transform to reference signal and the measured image signal respectively, and get the phase information in the frequency field according to the real part and imaginary part of the signal, namely get the distance between the measured target and the camera for each pixel point according to the phase difference of the both. For the image conversion, the required calculation work is quite large to conduct fourier transform for the iamge directly, so use fast fourier transform (FFT) to conduct data treatment.

Use fourier transform to convert 2D image from time domain to frequency domain, basic formula as follow:

$$F(u,v)=\frac{1}{N}\sum_{x=0}^{N-1}\sum_{y=0}^{N-1}f(x,y)\exp[-\frac{j2\pi(ux+vy)}{N}],u,v=0,1,\ldots,N-1 \qquad (1)$$

Use fourier transform to convert 2D image from frequency domain to time domain, basic formula as follow:

$$f(x,y)=\frac{1}{N}\sum_{u=0}^{N-1}\sum_{v=0}^{N-1}F(u,v)\exp[\frac{j2\pi(ux+vy)}{N}],x,y=0,1,\ldots,N-1 \qquad (2)$$

In order to weigh distortion degree of image color, this paper compared the color differences by calculating the color differences in CIELAB color space between the collected image and original image. See color differential calculation in formula 3, where, *abΔE (x , y) is the color differences among images, see calculation method in formula 4. If the closer color differences closer to 1, image color differences are smaller.

$$e(x,y)=1-\frac{1}{255\sqrt{3}}\Delta E^{*}_{ab}(x,y) \qquad (3)$$

$$E^{*}_{ab}(x,y)=\sqrt{(L^{*}_{x}-L^{*}_{y})^{2}+(a^{*}_{x}-a^{*}_{y})^{2}+(b^{*}_{x}-b^{*}_{y})^{2}} \qquad (4)$$

$L^{*}_{x}\ a^{*}_{x},b^{*}_{x}$ and $L^{*}_{y},a^{*}_{y},b^{*}_{y}$ are the corresponding dimensionality of brightness and color in CIELAB color space for image x and image y respectively.

Based on FFT structure of data flowing mode allowing data continuously to input to FFT engine, it can output plural data flowing on FFT output interface continously without blocking data flowing. When the system reset signal drawing high, data source (can be FFT engine module) will draw sink_valid signal high to instruct that input interface can be used. When both of sink_valid and sink_ready signals are effective, it shows data is transmissing successfully. After data transmission completed, sink_stop signal will draw low, and the sampled data will be put in natural sequence. When the last sampled data is loaded, data source will draw sink_eop and sink_valid signals high to instuct the last data finishing transmission. See the simulation waveform of outputting FFT engine in the figure, from the simulation figure, FFT engine can continously respond to the input data flowing and output plural data on the output interface.

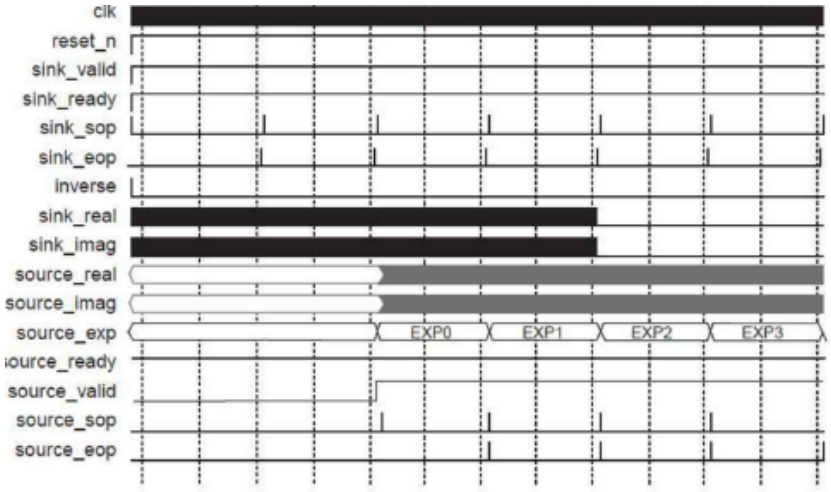

Figure 7 Simulation Waveform of FFT Flowing Data Structure

Based on the accuracy of time sequence simulation and the necessity of using ModelSim simulation when designing FPGA, the designer can be separated from practical hardware development environment and completely use computer to conduct simulation design, which improves the desinging efficiency of the engineers and also cuts down the designingtime and the time for product to market. See the conversion example of image FFT in the figure.

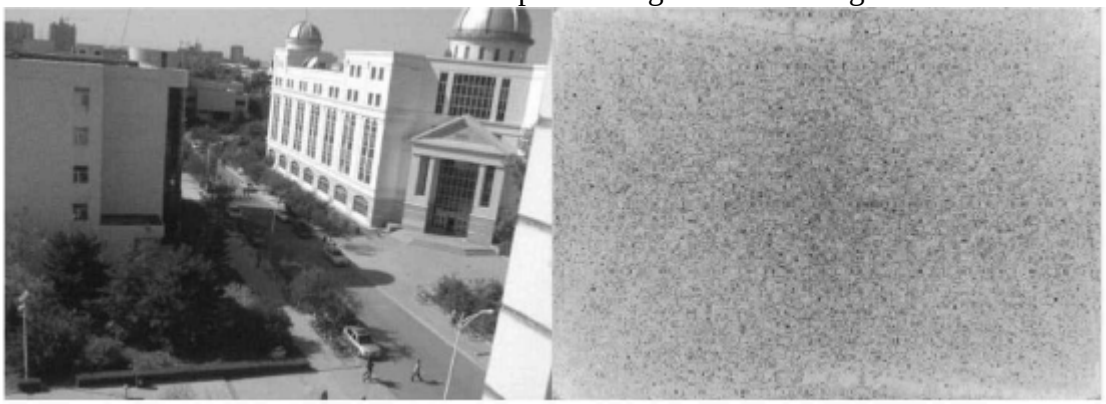

Figure 8 Conversion Example of Image FFT

Summary

This paper introduced the overall designing plan, which is based on the medical endoscope picture pick-up system of ARM and FPGA, studied the realization method of communication between ARM and FPGA as well as realized drive program development of ARM and FPGA communication interface. Moreover, it realized both communications taking FPGA as the peripheral storage device of ARM by system bus connecting to ARM. Study result showed that this system realized the functions of image freeze, image playback and real-time display, and also realized the transmission of freeze image from FPGA to ARM. Such system accounting for small amount of FPGA resource provided hardware platform for follow-up image treatment and development with the characteristics of small volume, low cost, simple circuit structure and designing flexibility.

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