

## Research and design of high precise adjustable power supply device

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**Abstract.** This paper research and design a precision adjustable power supply. The voltage in the range of 3.3V to 3.4V, the ripple voltage and its peak value of not more than 100mV, power is about 1W, the power supply can be provided to the optical module, its security is good, and can support the RF device, the power supply starting surge voltage time close to 0. In the choice of method of removing surge ripple, designed a rated output voltage 5V, rated output current of 1A low dropout linear regulator (LDO), the device is compared to the DC/DC circuit, effectively reducing the ripple. By experimental verification, the design scheme is feasible, and has good application value.

### Introduction

With the rapid development of information science technology, power supply becomes more and more important. Especially low voltage stabilized power supply more popular in intelligent instruments and today, more and more extensive application, low voltage stabilizing circuit so the research and design of adjustable power supply technology, become the focus again in the. In recent years, with the development and application of sensor technology, optical module is used more and more in the sensor circuit, driving the light module of the power supply requirements of high stability, and the price is expensive, the voltage fluctuation exceeds a certain range, it is easy to burn<sup>[1,2,3]</sup>, Therefore, in this paper a technique parameters in the drive voltage of between 3.3V-3.4V, optical module and ripple peak voltage should not exceed 100mV, the design of adjustable power supply, a high precision. The ripple power to remove the circuit using LDO, which has a small volume, high power supply rejection ratio, low power consumption, low noise and the advantages of simple circuit application end, in addition, LDO also has a good linear transient response and load transient response, complete the design of the high precision adjustable power supply can provide light module in 25GHz, security is good, can support the RF device, and the power supply startup surge voltage close to 0.

### The design of LDO device

LDO consists of a current source, voltage reference, error amplifier, adjust the tube and a sampling circuit, the design of the power performance requirements of rated voltage 5V, output current 1A; power measurement module circuit signals are input to collection points magnification, A/D conversion module and then input to the STC12C5A60S2 SCM, the analog signal is converted to digital signal [6], and then through the single-chip power calculation, through the liquid crystal display power; leakage protection module input the signal acquisition to the amplifier circuit, signal amplification, two ways of signal amplification signal output by control RS trigger is more amplified, control relay drive circuit, the realization of leakage protection and automatic cutting. The schematic diagram shown in Fig. 1.

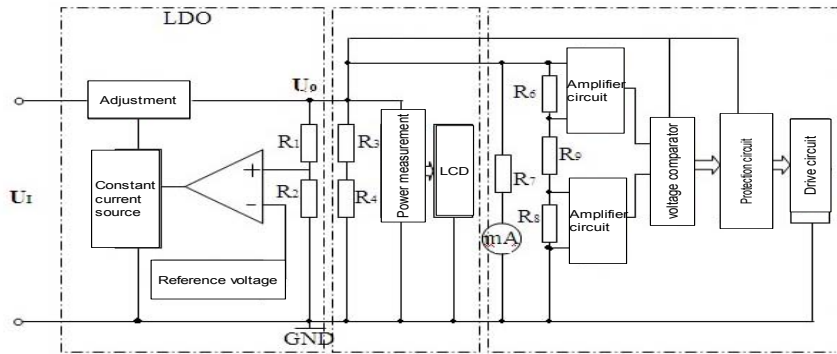


Fig.1 Block diagram of LDO system

### LDO Unit circuit design

The power from the constant current source (the core components for the PNP pipe, NPN pipe, Q1 voltage reference (Q2) voltage regulator tube, an error amplifier (D1) integrated operational amplifier (OP295), adjusting pipe (two PNP tubes Q4 and Q5) and a sampling circuit, reached the rated voltage 5V, output current performance requirements 1A. The sampling voltage is applied on the in-phase input terminal of the comparator OP295, compared with the added to the inverting input terminal of the reference voltage  $U_z$ , the difference between the two after the amplifier amplified OP295 series adjustment, control pipe pressure drop, and thus the stability of the output voltage. When the output voltage of  $U_{out}$  is reduced, the difference between the reference voltage and a sample voltage increases, the comparison amplifier output driving current increase, series adjusting pipe pressure drop decreases, so that the output voltage rise. On the contrary, if the output voltage exceeds the set value of  $U_{out}$  required, comparison amplifier out put front drive current is reduced, thereby reducing the output voltage. The specific circuit as shown in Fig 2.

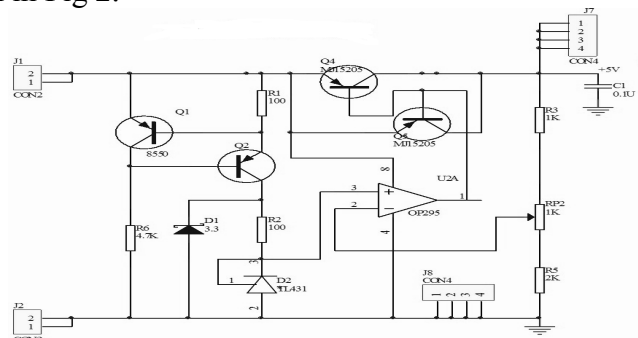


Fig. 2 LDO unit circuit

### The design of the adjustable voltage unit circuit

Fig. 3 is the adjustable voltage unit circuit, are the input and output of rail2rail, so as to ensure maximum adjustable range. One way is to be transferred to the 5V, so that the sliding way and a resistor string, to ensure that such plus electrical output in 5v5 is also less than 5V, because generally lowered the rarely used 5V voltage, so the voltage lower than 5V has little.

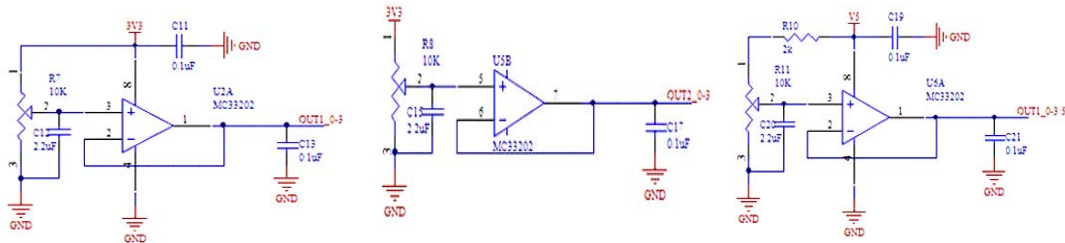


Fig. 3 adjustable voltage unit circuit

### Anti surge and protection circuit design

In the circuit surge related to the success or failure of the design, in general, is a good method to solve the surge of LDO soft start, but in order to design the universality, the chip does not support soft start condition, can use RC hardware delay or in the chip itself enable terminal output will be delayed by the absence of elevated Saint using TVS, protection and prevent high voltage protection measures. In this design, according to the relevant technical parameters by a chip, the attention paid to the manual chip in enable pulled after the delay, output increased slowly (about 0.1ms), as shown in Fig.4. In order to guarantee the delay to meet the surge time requirements, at the end of the input string into a Schottky diode and self recovery fuse TVS protection, as shown in Fig. 5.

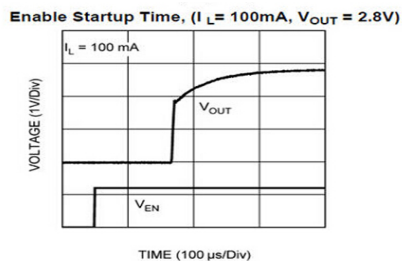


Fig. 4 output voltage that can pull up after

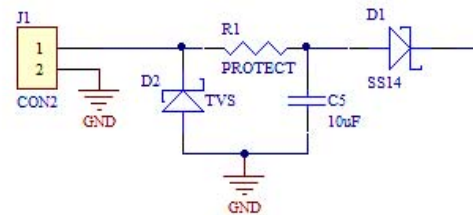


Fig. 5 TVS protection circuit

The LDO input voltage can not be too 5.5V. So at the input to the protection circuit design , as shown in Figure 6 circuit design. Among them, the voltage reference output 3.0V standard reference, the reference voltage will need very accurate, a reference voltage application comparison should be using the same package LDO. Another way is the actual voltage divider, when the input is below 5.5V, the comparator output low level, the switch tube conduction, otherwise, the negative input end of the comparator is higher than the closed, tube short, so as to ensure the safety of the circuit. In the choice of operational amplifier, graph Potter needs to contrast diagram and chip manual, the load capacitance is not too large, such as phase condition is not satisfied, the chip will produce began to self.

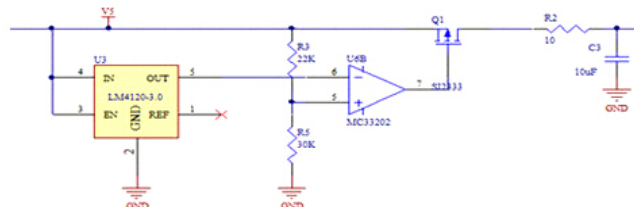
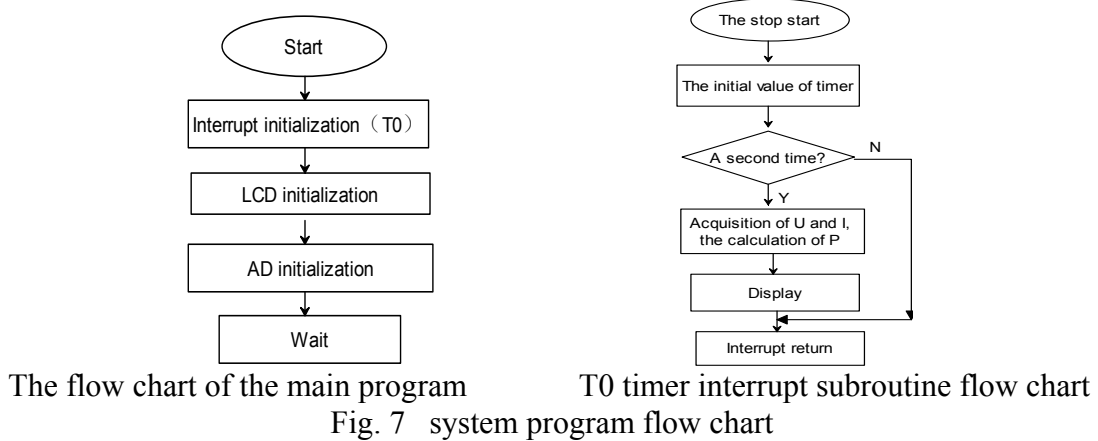


Fig. 6 protective circuit diagram

### The software design of the system

The main program mainly on AD , timer initialization. AD STC 12C5A60S2 comes with AD analog voltage acquisition, and converted to the actual voltage, current by calculating the Ims timer; timing, each interrupt counting, counting to 1000 times for 1S, this time through the AD converter collection Uout, and Iout, and the calculation of instantaneous power, at the same time to

send LCD display. Data acquisition frequency is 1HZ. The program flow chart as shown in Fig. 7.



### The test results and conclusions

This article through the design of the LDO, and the basic design of a voltage in the 3.3V - 3.4V, the ripple peak power less than 100mV, in 1W, can provide the optical module, the security is good, can support the RF devices and power supply startup surge voltage close to high precision 0 adjustable electrical source. The design of LDO, to some extent alleviated the surge voltage, and then the subsequent processing, using the delay parameters of the device itself, the corresponding protection circuit design, a good solution to the current surge. After the test, the voltage fluctuation range between 3.30V-3.37V, as shown in Fig. 8, the ripple voltage is less than 70mV, very good to achieve the design requirements.

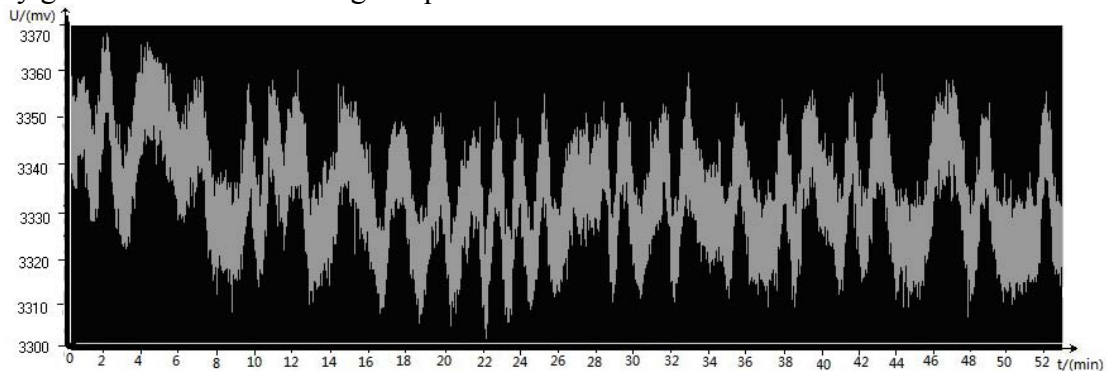


Fig. 8 measured voltage to ripple

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