Research of the distributed power system dynamic voltage restorer simulation based on DSP

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Abstract. This paper aims to design a distributed grid simulation system dynamic voltage restorer means to solve the problem of dynamic energy security in case of equipment operating in the electricity voltage sag or interruption. Means the use of "DC - AC" and "AC - DC - AC" dual structure, control system uses TMS320F28335 to control core sampling method within the rules and DSP chip EPWM module functions to achieve SPWM wave, after hardware and software design, the test of the PFC link device, the power factor was close to 1; a small error SPWM modulation algorithm approximation introduced DC voltage fluctuation detection circuit and AD converter error. POST, input under-voltage and output over-current protection, over-current, under-voltage troubleshooting can automatically restore.

Introduction

In this paper, a dynamic voltage restorer experimental device, a "DC - AC" and "AC - DC - AC" dual structure, the first stage power factor correction (PFC) circuit, its role is to complete the AC - DC conversion,It can improve the input side of the power quality. The second stage is a single-phase full-bridge inverter topology plus output transformer. Full-bridge inverter control through DSP dead zone control, to prevent direct access for distributed grid dynamic voltage restorer analog system.

1 Overall program

DVR topology shown in Fig. 1. It mainly consists of the active filter and the inverter device, DVR and the inverter device, constitute the critical load. Energy storage unit and a two-stage public interface, the system is running, if the voltage is normal, DVR devices do not compensate for the amount of voltage to the injection system, the device itself is very low power consumption in the standby state. When the dynamic voltage drop and other problems arise, DVR means instant start, to put the circuit compensation, ensure that the voltage is normal. When the voltage is restored, DVR device back to standby.

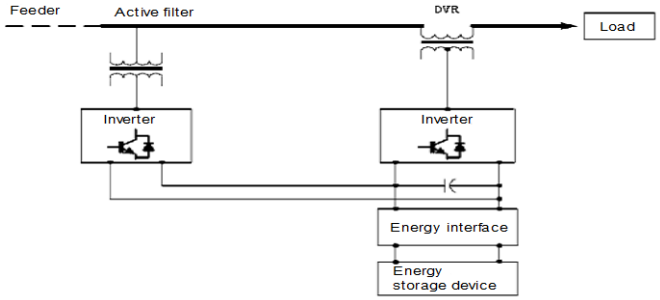

Fig.1 DVR topology

Design uses TMS320F28335 as a controller, which has a programmable dead-time control function, which prevents bridge driver circuit to produce upper and lower leg straight and burned. At the same time can generate SPWM signal to generate SPWM waves through regular sampling method, the symmetry regular sampling algorithm is shown in Fig. 2. Fig.2 can be obtained:

$$\begin{cases} t_{off} = \dfrac{T_s}{4}\left(1 - M\sin\omega t_1\right) \\ t_{on} = \dfrac{T_s}{4}\left(1 + M\sin\omega t_1\right) \end{cases} \quad (1)$$

The Pulse width:

$$t_{pw} = \frac{T_s}{2}\left(1 + M\sin\omega t_1\right) = \frac{T_t}{2}\left(1 + M\sin\omega t_1\right) \quad (2)$$

Formula (1), the sampling points. (2), the sampling point in time only to carrier ratio,whereas the ratio has nothing to do with the amplitude modulation, and:

$t_1 = kT_t, k = 0,1,...,N-1$。

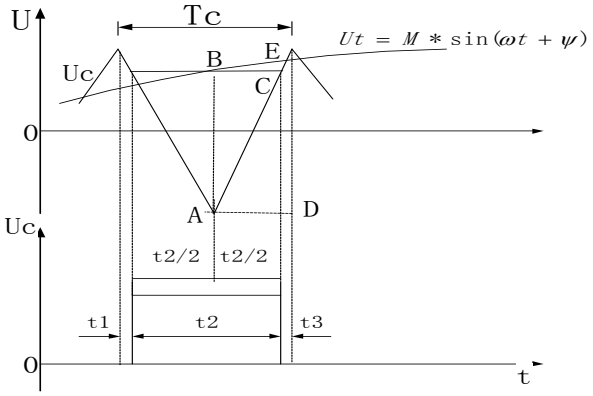

Fig. 2 A schematic symmetry regular sampling algorithm

2 PFC control method

System control mode uses average current mode Boost PFC calculated directly from the PFC control circuit parameters are given initial PWM waveform, when the system starts, PI current loop be adjusted, in the realization of the system fast start also avoid starting inrush current sampling noise. In addition, the system samples the moment of starting the input current waveform, while closed-loop control, precise tracking phase, significantly reduce the current distortion.

3 The Hardware Design

3.1 Inductor current conditioning circuit

Input current conditioning circuit shown in Fig.3. Design uses a resistor current into a voltage signal, and then by the INA282 will pass active filter into the DSP signal amplification after sampling.

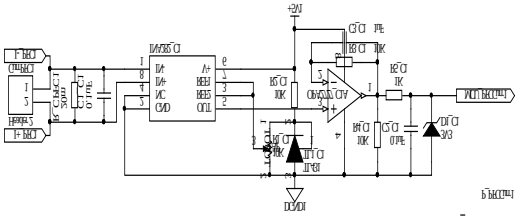

Fig. 3 input current signal conditioning circuit

3.2 PFC input voltage frequency detection circuit

The frequency of the input voltage detection circuit shown in Fig.4. First, the input signals using transformer isolation, after a zero comparison and plastic limiter get square wave signal, based on the characteristics of DSP, ECAP captured on the rising and falling edges of the signal only in response to the module, and the amplitude of the signal equally strict requirements (less than

3.3V), and therefore need sinusoidal signal output into a square wave signal is less than the amplitude of 3,3V, in the zero crossing, in order not to cause false triggering CAP, zero-crossing switching signal is necessary to avoid oscillation.

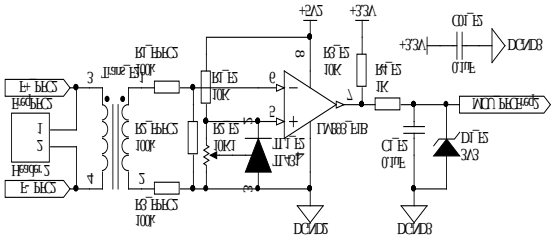

Fig.4 Input voltage frequency detection circuit

3.3 DC voltage and current conditioning circuit

DC voltage signal conditioning circuits, and DC current signal conditioning circuit, respectively, as shown in Fig. 5 and 6. DC voltage across the resistor divider, is followed by a voltage through the low-pass filter into the sampling. DC current signal is fed through a resistor converts the sampled signal into a voltage signal is amplified by an amplifier voltage.

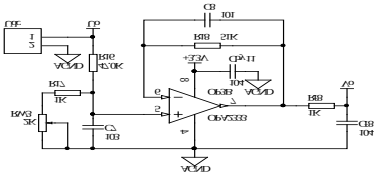

Fig.5 DC voltage signal conditioning circuit

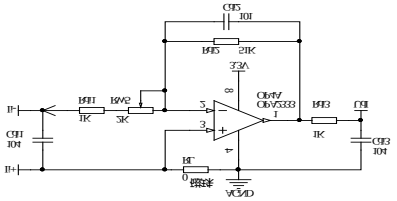

Fig. 6: DC current signal conditioning circuit

4 Testing and Conclusion

4.1Frequency tracking range test

Test method: When the system is working at UPS status, input standards vary between 40Hz-60Hz sine wave test output voltage frequency. The test results are shown below.

Source Frequency(Hz)	41.987	48.667	50.001	56.325	60.010
System output frequency(Hz)	41.863	48.644	49.983	57.432	59.987

4.2 Output voltage accuracy test

Test mode: Set the output voltage of 10V and 20V, respectively, under the circumstances, in order to adjust the size of the load change from 10Ω-30Ω measuring voltage stabilization accuracy. Regulation accuracy of test data in the table below, showing the system stable within 1%.

Load size	10Ω	15Ω	20Ω	25Ω	30Ω
Set the output voltage of 10V size	9.99V	9.98V	10.02V	10.05V	10.06V
Set the output voltage 20V	9.91V	9.94 V	9.96 V	10.00V	10.01V

4.3 PFC input power factor and waveform distortion measurement

Enter the job at PFC modes, respectively, under different load conditions, power factor and waveform distortion test data obtained in the table below, it can be seen from the table, power factor close to 1, waveform distortion rate.

Input Current	2A	1.5A	1A	0.5A
Power Factor	0.97	0.99	9.98	9.98
Waveform distortion rate	5%	3.1%	2.1%	1.0%

5. Conclusion

After more than hardware and software design and test test test frequency tracking range, the output voltage accuracy test, PFC input power factor and waveform distortion measurement, the error is within the allowable range. In the PFC link, the power factor was close to 1.

For maximum frequency point tracking function, not by changing the source impedance and load, the relative deviation test was very small, the absolute value of only 0.6%.

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