Design of the acquisition system of Spread-spectrum TT&C signal

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Keywords: Spread and control; rapid capture; Field compiled.

Abstract. **A**n acquisition algorithm of Spread-spectrum TT&C signal is studied in this paper. The theory and key technology is analyzed. The block of design and the scheme of program are presented. The processing system of Spread-spectrum TT&C signal is actualized by the FPGA, and the function of the fast acquisition of Spread-spectrum TT&C signal is implemented.

1. Introduction

And control the spread and control is a way to have a very excellent performance since its birth on the subject of widespread concern, and to capture and control the spread spectrum signal occupies an important position in the overall system implementation. The traditional serial pseudo-code spread spectrum signal acquisition algorithm [1-4] due to capture slow, has been unable to meet the actual needs of measurement and control systems, and therefore to design a suitable environment for the measurement and control the spread and control signal acquisition scheme, will have a certain the project value and practical significance.

2. Parallel acquisition algorithm based on cyclic-related pseudo-code

The traditional serial pseudo-code spread spectrum signal acquisition algorithm using pseudo-code serial sliding due to the way to achieve the initial phase of the pseudo-code searching, capturing a long time. Pseudo-code from the capture process to analyze, if we can simultaneously search all of the code phase unit, the acquisition time will be significantly reduced. To search all of the code phase cell cycle in a pseudo-code is required to move the local loop pseudo code phase correlation with the received pseudo-code, when the phase of the local code and the code exactly as you receive the greatest correlation peak volume of this cycle form can be expressed as the product of:

$$s(n) = \sum_{i=0}^{N-1} r(i)c(i+n) \quad n = 0,1,2,N-1 \qquad (1)$$

Formula (1), in order to receive the pseudo-code; local pseudo-code; adjusted to traverse a number of cycles needed for the pseudo-code. Obviously, if the direct calculation of the equation, the calculation is very large, proportional. It is found that the formula (1) may form the following matrix:

$$\begin{bmatrix} s(0) \\ s(1) \\ \cdots \\ s(N-1) \end{bmatrix} = \begin{bmatrix} c(0) & c(1) & \cdots & c(N-1) \\ c(1) & c(2) & \cdots & c(0) \\ \cdots & \cdots & \cdots & \cdots \\ c(N-1) & c(1) & \cdots & c(N-2) \end{bmatrix} \times \begin{bmatrix} r(0) \\ r(1) \\ \cdots \\ r(N-1) \end{bmatrix} = \mathbf{CR} \qquad (2)$$

Formula (2), the matrix C from the first row, sequentially moves one element, the elements move out of the next line appeared. So you can use the principles of time-domain circular convolution is equivalent to multiplying the frequency domain, time domain acquisition pseudo-code can be transformed to the frequency domain using the FFT to the quick search code phase, relatively straightforward calculation, this will significantly reduce the computational complexity and computation time. The mathematical principle as follows:

$$s(n) = \sum_{i=0}^{N-1} r(i)c(i+n)$$

$$= \sum_{i=0}^{N-1}\left[\frac{1}{N}\sum_{k=0}^{N-1} R(k)\exp(j\frac{2\pi}{N}ki)\right]\left[\frac{1}{N}\sum_{l=0}^{N-1} C(-l)\exp(-j\frac{2\pi}{N}l(i+n)\right]$$

$$= \frac{1}{N}\sum_{k}\sum_{l} R(k)C(-l)\exp(j\frac{2\pi}{N}lk)\frac{1}{N}\sum_{i=0}^{N-1}\exp[j\frac{2\pi}{N}(k-l)i] \quad (3)$$

Due to $$\sum_{i=0}^{N-1}\exp[j\frac{2\pi}{N}(k-l)i] = \begin{cases} N & k+l=0,N,2N,\cdots \\ 0 & others \end{cases} \quad (4)$$

Therefore, equation (4) can be obtained

$$s(n) = \frac{1}{N}\sum_{k=0}^{N-1} R(k)C(-k)\exp(j\frac{2\pi}{N}kn)$$

$$= IFFT\{FFT(r(i)\times FFT^{*}(c(i)))\}$$

(5)

Wherein, respectively, the frequency-domain value. And because its signal cycle characteristics, you only need to make the point FFT can achieve a pseudo code phase traversal, and estimate the frequency spectrum of the signal will not be generated aliasing distortion.

Spread and control signals in the initial acquisition, tracking unfinished due to the angle so that the received signal to noise ratio are relatively low, in a pseudo-code cycle coherent integration of spreading gain is insufficient to meet the actual requirements. \So consider using part of the matched filter (non-coherent accumulation) with increased frequency division groove combination system processing gain, in order to meet the dynamic needs of the low SNR capture and control. Circular correlation based on the FFT algorithm, shown in Figure 1, non-coherent accumulations by K times, can effectively improve the system processing gain.

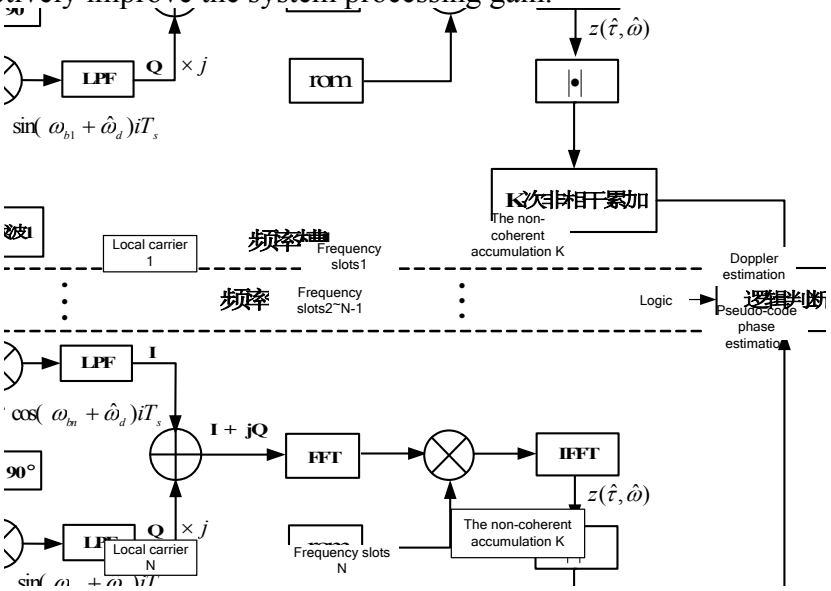


Figure 1 FFT algorithm based on a block diagram of the cycle-related

3. Further Algorithm

The algorithm in the actual process, the value of the receiver via a local spreading sequence for the FFT is first stored in rom in order to reduce local pseudo-code for the FFT and the pressure to the hardware resources. The pseudo-code in order to make and receive local relevance optimal pseudo-code, you should take a symbol of an integer number of sampling points. At the same time bring a contradiction is, in pseudo-code sequence spread spectrum signal is generally, but the optimal operation of FFT radix-2 or radix-4, which points to an integer power operation 2 or 4. By spreading the received signal cycle zeros, can effectively solve this conflict.

But for a pseudo-code cycle zeros, may undermine the entire pseudo-code sequence correlation, the correlation value zeros by equation (6) is obtained.

$$\begin{bmatrix} s(0) \\ s(1) \\ \cdots \\ s(N) \end{bmatrix} = \begin{bmatrix} c(0) & \cdots & c(N-1) & 0 \\ c(1) & \cdots & 0 & c(0) \\ \cdots & \cdots & \cdots & \cdots \\ 0 & c(0) & \cdots & c(N-1) \end{bmatrix} \times \begin{bmatrix} r(0) \\ \cdots \\ r(N-1) \\ 0 \end{bmatrix} \quad (6)$$

Figure 2 can be performed after the analysis by the formula (6) decomposition.

As can be seen from Figure 2, in a pseudo-code cycle zeros may destroy the original spreading sequence.

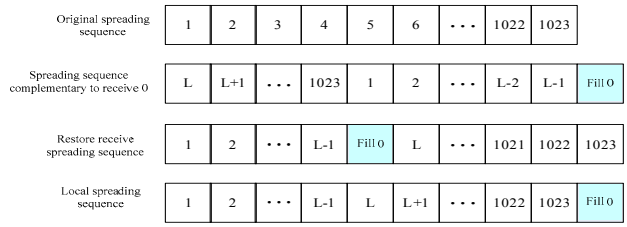
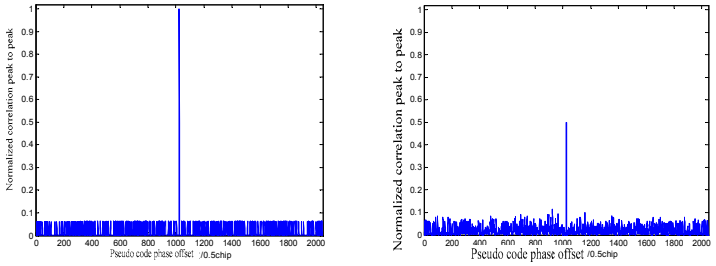


Figure 2 A schematic diagram of the pseudo-code period up to zero after

In the worst case, the receiving PN and local pseudo-code in one cycle will be half of the number of pseudo-code is not on, that is related to the energy loss of about peak.



(a) Correlation peak prosequence (b) pseudo-code zeros after cycle correlation peak

Figure 3 compares the correlation peak of a pseudo-code cycle zeros

As shown in Figure 3, the simulation conditions, the pseudo-code to receive the local pseudo-code delay than half a pseudo-code cycle. Figure zeros can be seen at the end of a serious impact on the pseudo-code correlation. Considering the problem, thus further conversion of the formula (6).

The simulation shown in Figure 4. Although a serious impact on the end of zeros Correlation two pseudo-code cycle, but a correlation between the first pseudo-code cycle was completely preserved, and therefore does not affect the accumulation and detection of the signal energy.

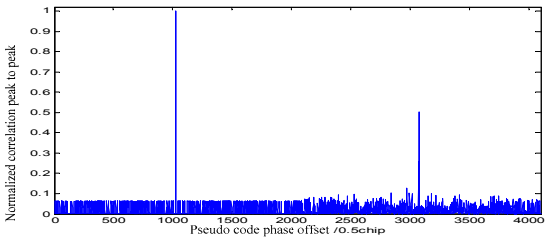


Figure 4 pairs of two pseudo-code period after the end of zeros correlation diagram

4. Algorithm Design and Implementation of FPGA-based

FPGA using Stratix II EP2S60F1020I4 bulk field programmable gate arrays. Its system is a major design concern is how to achieve the received signal FFT with local storage rom the two-way data synchronization input. If the received signal a FFT calculation cycle fails to synchronize with the local rom the data output cycle, the overall result of the operation will be unpredictable. Therefore, the system is designed to effectively utilize the output of the FFT operation before they can trigger addressable modules for signal synchronization signal. The principle shown in Figure 5.

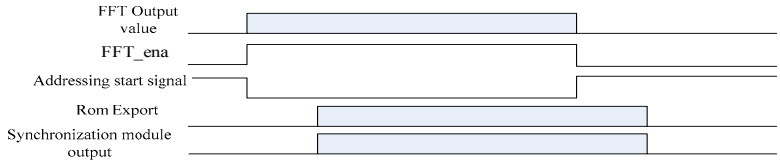


Figure 5 FFT output synchronous signal control and rom

When the FFT computation module output operational value, while the output value of the available signal FFT operation FFT_ena, the use of the control signal is negated after addressing module work, and synchronization module for FFT output value is latched and begins counting. When after n clock cycles later, Rom starts to output, the synchronization module also starts to output.

Vector Waveform use static simulation performance tests:

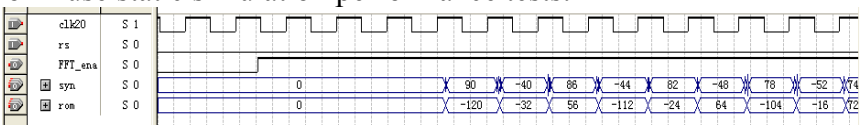


Figure 6 a schematic view of the synchronization control module emulation

Which, syn, rom rom respectively synchronization module and memory modules all the way to the signal output value. As can be seen from Figure 6, the synchronization module output syn signal output rom rom memory modules to achieve a synchronization signal output, to meet the design requirements.

When the received signal is FFT operation is completed, after the local rom synchronization signal, the need for multiplying two complex signal processing, according to the formula

$$(a+bj)\times(c+dj)=(ac-bd)+(ad+bc)j \quad (j \text{ for complex symbols}) \qquad (8)$$

Can be deduced by four signals were doing multiply, multiply complex multiplication subtraction can be realized. And then the two output values of the inverse FFT operation once the completion of the relevant accumulation operation cycle.

5. Algorithm performance testing

5.1 Program test

Simulation conditions: Pseudo-code length bits, pseudo-code rate 10.23Mchip / s, the received signal carrier with a local carrier frequency difference of 500Hz. System sampling rate 102.3MHz, after low-pass filtering down-converted five times extraction, the system processing rate drops 20.46MHz, for the 4096-point FFT on the signals and the corresponding inverse transform, which captures the results shown in Figure 8 (using the track rising edge triggered):

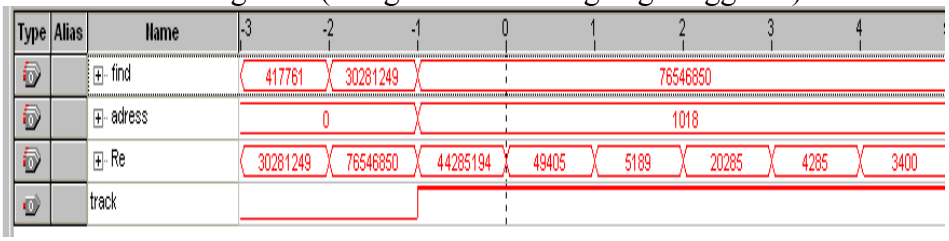
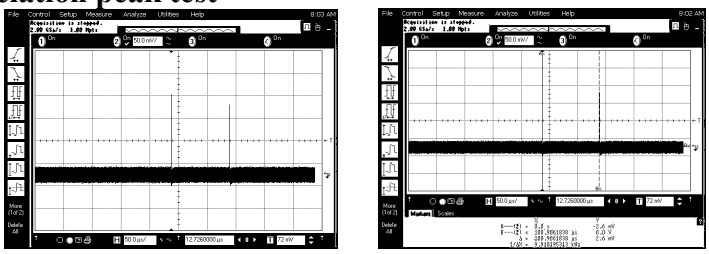


Figure 7 SignalTap Ⅱ schematic simulation

As can be seen from Figure 7, when fft peak output exceeds a threshold, track the output signal capture, address output 1018, is the local pseudo-code and pseudo-code of the receiving phase. By adress signal to the local pseudo-code generator an initial phase, the local pseudo-code generator start control system to complete pseudo-code capture process.

5.2 Pseudo code correlation peak test



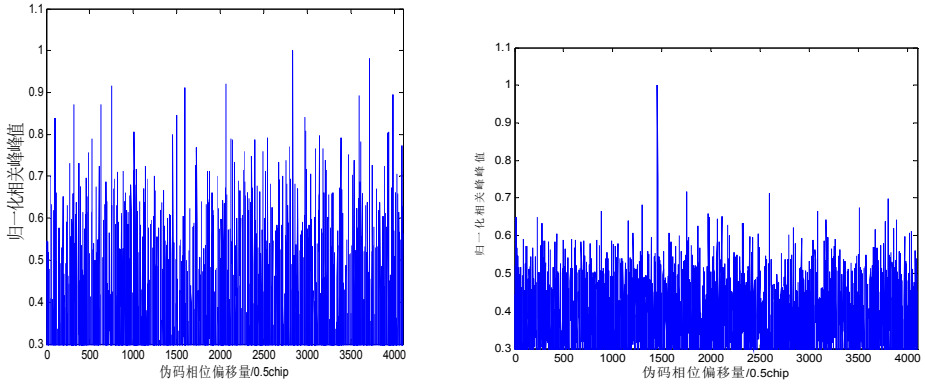
(a) Test correlation peak (b) the correlation peak test (using the ruler measurements)

Figure 8 pseudo-code correlation peak test

Figure 8 is the use of Agilent 54853A DSO oscilloscope test fast FFT of the carrier to noise ratio 45dB-Hz spread spectrum signal, after 300 iterations output value calculation. Consistent with the results of the design, the output correlation peak for two cycles, Figure (b) it can be seen as the interval between the two relevant, just as a pseudo-code period, to prove the correctness of the output result.

5.3 Non-coherent integration and frequency slots influence and control signal acquisition performance testing

IF carrier set to 70MHz, sampling rate of 102.3MHz, code length bits, pseudo-code rate 10.23Mchip / s, extractor factor is set to 5, then each pseudo-code period after downsampling sampling points for AA, using the FFT algorithm pseudo code parallel acquisition, the accumulation of the two pseudo code period after zero padding 4096 points FFT computation is divided six frequency bins, the effective range of each frequency bin is, the search for a total frequency range. Doppler shift of the received signal to 25.1KHz, pseudo code offset 500 points (approximately), carrier-to-noise ratio of 45 (dB-Hz). In the closest Doppler shift groove, i.e., the Doppler frequency deviation of 100Hz groove simulation results shown in Figure 5 (not in the 1546 point estimate because downconverted delay effect caused by the low-pass filter) .



(a) non-iterative (b) 50 times iteration

Figure 9 Relations with non-related cumulative frequency correlation peak

The simulation can be found in the relevant FFT algorithm based on cycle through improved design, fully meet the monitoring and control of the spread spectrum signal is a pseudo-code acquisition.

5.4 Capture time test

Table 1 circular correlation algorithm capture time (unit / s)

Experiment / Frequency / CNR（dBHz）	***1***	***2***	***3***	***4***	***5***	***6***	***7***	***8***
55	*0.044*	*0.044*	*0.044*	*0.044*	*0.044*	*0.044*	*0.044*	*0.044*
52	*0.044*	*0.044*	*0.087*	*0.044*	*0.044*	*0.044*	*0.044*	*0.044*
48	*0.053*	*0.053*	*0.053*	*0.053*	*0.053*	*0.053*	*0.053*	*0.053*
45	*0.061*	*0.061*	*0.122*	*0.061*	*0.061*	*0.122*	*0.061*	*0.061*

Table 1 shows the pseudo-code parallel search algorithm test of time. Table 45dB-Hz 6th capture long time due to an adjustment in the first pseudo-code and the next phase of the cycle does not capture a pseudo code adjustment cycle capture. Table 52dB-Hz 3rd, 45dB-Hz 3,6 times the data acquisition time is longer due to the accumulation of the signal transition impact and capture the next cycle.

6. Conclusion

The design principles and key technologies spread spectrum telemetry signal acquisition is proposed overall design diagram and program design, and the use of Alter's Stratix II family EP2S60F1020I4 chip testing program, the successful implementation of the monitoring and control signals between the actual measurement experiments, with a spread quickly capture and control signal functions. With the completion and operation of the new generation and control system, to improve the ability to capture and control system has certain significance.

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