Communication of double TMS320F28335 DSP Based on McBSP

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Abstract. A bidirectional real-time data communication without distinction between master and slave is achieved with double TMS320F28335 DSP using its multichannel buffered serial port (McBSP). The shortcoming of the communication on SPI mode that the slave cannot initiate communication is overcame. The hardware connection and the software realization plan of the scheme are detailed. Finally, tests on uninterruptible power supply (UPS) inverter prototype controlled by double TMS320F28335 DSP verify the reliability and real features of this design.

1. Introduction

With the outstanding point of the high speed and good precision of its processing capacity and the rich internal and external resource, as well as the flexible connector and the higher cost performance, Digital Signal Processor(DSP) is widely applied into communications, digital image processing, industrial measurement, control and electrical home appliances and other fields[1] . However, in some practical industrial application, the only use of single piece DSP can't come to reach the requirement of the systematic design owing to the large data collection and processing. Thus, it asks for the inter-connection of two pieces or more pieces of DSP to achieve the coordinate work of the whole system[2]. Therefore, it's especially important to research on the high-speed, real-time and reliable communication between DSPs.

TMS320F28335[3]is a new launch of Texas Instruments(TI), which is a 32-bits floating DSP with low consumption and high performance. This paper researches on the method by adopting the McBSP module of TMS320F28335 to realize the high speed and real-time communication between double DSP. And combined with the practical application, the paper produces a bidirectional real-time communication scheme without the master-slave relationship, which hereinafter is called NSPI communication solution for short. This scheme overcomes the shortcoming of unable to take the initiative communication under the model of SPI communication and is successfully applied into the control system of UPS.

2. Dual DSP System Communication Method

In the dual DSP communication system using the McBSP module, a common communication method is a master-slave way, that is SPI communication [4,5]. SPI communication has a master device in charge of the distribution of task scheduling in the whole system and human-computer interaction and a slave to share the data processing task of the master device and sent the processing results back to it. In this process, McBSP serves as the slave, which only needs to write and sent to the register first before sending to the main engine and then it's not until accepting the control signal coming from the master device that can send the data to master device.

SPI communication method is applicable to parallel processing system when the real-time demand of sending data from slave device to master device is low, while it can't reach the requirement when applied to dual processor peer-to-peer communication occasions. Owing to the interior structural features of McBSP module, it not only can take the SPI communication method, but also realize communication without a master-slave full-duplex when adopting the McBSP to achieve double DSP communication, which is called NSPI communication for short.

3. Hardware Interface of Dual DSP and Data Transfer Process

The interface connection diagram to realize dual DSP communication by adopting McBSP as shown in Figure1. There are two McBSPs on the TMS320F28335 device, each of them consists of a data-flow path and a control path connected to external devices by six pins[3], namely data transmit (DX) pin, data receive (DR) pin, transmit clock (CLKX) pin, receive clock (CLKR) pin, transmit frame synchronization (FSX) pin, and receive frame synchronization (FSR) pin. When transmitting data, the CPU or the DMA controller writes the data to the data transmit registers (DXR1,DXR2). The data written to the DXRS is shifted out to DX via the transmit shift registers (XSR1,XSR2) . Similarly, receive data on the DR pin is shifted into the receive shift registers (RSR1,RSR2) .Once the full word is receive, the contents of RSRs are copied into the receive buffer registers (RBR1, RBR2). Finally, the contents of the RBRs is copied to the data receive registers (DRR1,DRR2), which can be read by the CPU or the DMA controller. If the length of the data to be transmitted or to be received is less than 16 bits, DRR2, RBR2, RSR2, DXR2, and XSR2 are not used. For larger word lengths, these registers are needed to be used to hold the most significant bits.

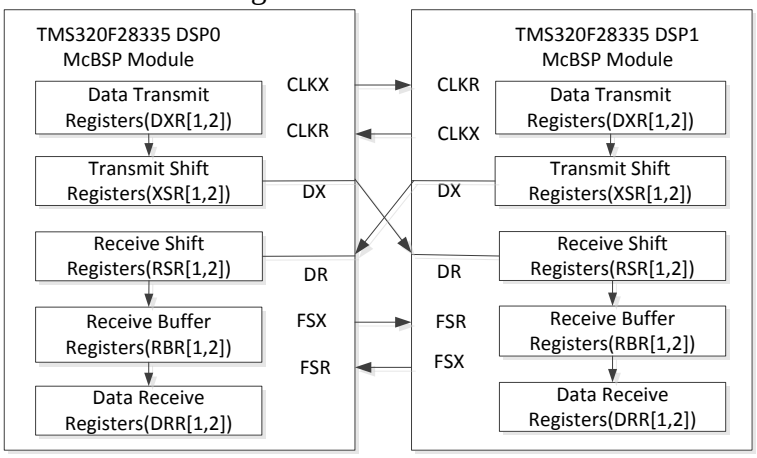

Fig. 1 the interface connection diagram under NSPI mode

It can be seen from Figure1 that McBSP module of TMS320F28335 has an independent data-accepting and sending shifting register and a buffer, so it can achieve the function without master-slave of the two pieces of DSP in McBSP module through reasonable configuration. Any one of McBSP can trigger the data sending and provide data accepting clock and control signal to the other one.

4. Software Design of NSPI Communication

The thought of the software design is described as follows. The sample rate generator within the McBSP module provides the sending clock in the module of DSP0. When the needed sending data in the DSP0 copies from DXR to XSR, it generates the sending frame synchronization pulse, which is set as the accepting frame synchronization pulse of DSP1. When the accepted data of DSP0 is copied from XSR to DRR, the receiver is ready to trigger the interruption of sign RRDY. Then it calls the interrupt service subroutine and reads data. The design of thought of DSP1 is also as well like DSP0.

In order to realize the software design of real-time communication between dual TMS320F28335 by adopting McBSP, it's essential to program DSP0 and DSP1, respectively. The key of design lies in the settings of related registers of McBSP. According to the design thought above, in the mode of NSPI communication, two pieces of DSP are with the same settings of McBSP related registers. The settings of the key registers are shown in Table 1.

The software design of two pieces of DSP consist of DSP initialization [6] (including the initialization of pin and interrupt vector, etc.), McBSP mode initialization, data-sending function and data-receiving interrupt functions. The software design flow schemes of data-sending and data-receiving are shown in Fig. 2 and Fig. 3, respectively.

Table1 the settings of key registers under the mode of NSPI communication

Control Bit	Set value	Set value
CLKSTP	00b	Non-SPI mode
CLKXM	1	MCLKR set as BIO,provided by the sample rate generator's internal clock signal CLKG
CLKRM	0	MCLKR set as BIO, driven by the external input clock signal
SCLKME	0	The clock of the sample rate generator is provided by the
CLKSM	1	systematic low-speed exterior clock LSPCLK
CLKGDV	0~255 arbitrary value	Define the division frequency coefficient of CLKG
FSRM	0	Accepting frame synchronization signal provided by FSR pin signal
FSXM	1	Sending frame synchronization signal provided by the interior sampling rate of generator
FSGM	0	When data copied from DXR to XSR,the sending frame synchronization pulse generates
RINTM	0	When the receiver's ready sign RRDY changes from zero to one, the interrupt signal RINT generates
RINT	1	Enable to receive interrupt signal

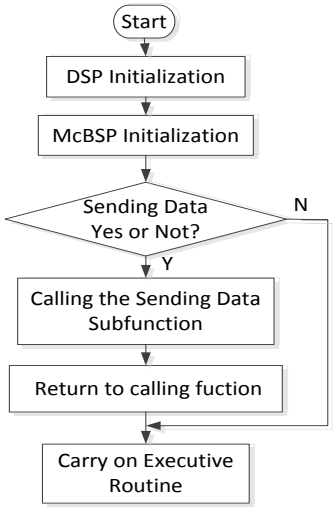

Fig. 2 Data sending flow diagram

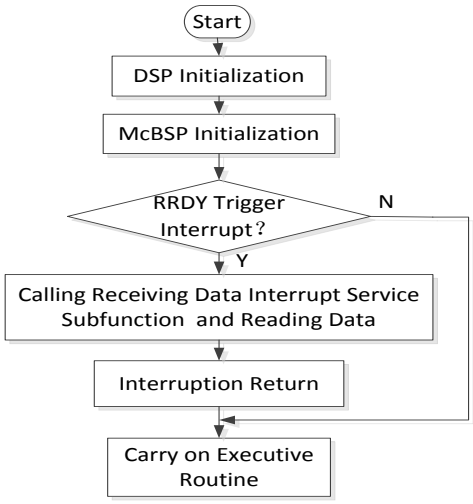

Fig. 3 Data receiving flow diagram

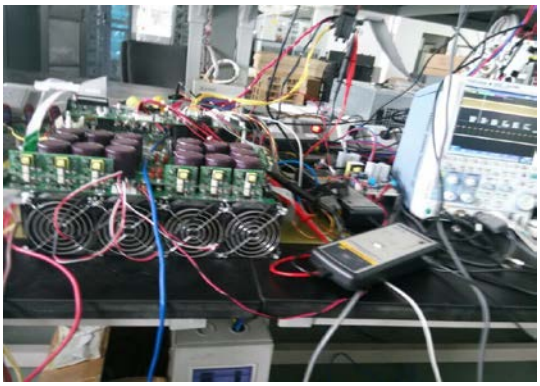

Figure4 the test bench of dual DSP

5. Experiment Method

According to the design procedure above, the experiment on the control panel of two pieces of DSP controlled UPS power module of rectifier and inverter is carried out. The test bench is shown in Figure4. The experiment methods are as follows. Turn on the DSP0 controlled control inverter in charge of the rectifier, after the successful turning on of the rectifier, it sends the boot demand to the control inverter DSP1. The results of the experiment show that the inverter is turned on successfully. Setting obstacles in the inverter, at the time of its power off, it sends the shutdown demand to rectifier. The outcome of the experiment shows that rectifier can be turned off successfully as well. In the experiment, the clock frequency of the McBSP is set as 4.6MHz, which indicates that two pieces of DSP both can independently control the sending of data and the other one can receive data accurately to realize the full duplex real-time communication at a high speed without master-slave.

6. Summary

Through the use of the McBSP module in the TMS320F28335 DSP, it can realize the simplicity and convenience of dual DSP communication hardware connectors without any external peripheral chips. This paper introduces the NSPI communication method to achieve the peer-to-peer communication between double DSP without the limit of main engine and slave in the SPI communication. The proposed scheme is successfully applied into the dual DSP control system with UPS rectifier and inverter. The system runs well which validate the feasibility and real-time of the designed scheme.

References

[1] H.G. Deng, B.D. Wang, J.N. Wu. Design and implement of double DSP communication based on CAN bus interface. Measurement & control technology,6:83-85,2011.

[2] W. Liu, Y.J. Lei, M. Mi. Application of software FIFO in communication of multi-DSP. Computer Engineering. 16:228-230,2005.

[3] Texas Instruments, TMS320F2833x/2823x Multichannel Buffered Serial Port(McBSP) Reference Guide,2011.

[4] W. Zhang, W. Liu, Z.H. Liu. High Speed Communication of Dual DSP Based on McBSP. Microcomputer Information,7:192-193,2008.

[5] Y. Song, H. Cai, S.X. Zhao. Implementation the Communication between DSPs by SPI Interface, Mechanical & Electrical Engineering Magazine, 5: 31-33,2005.

[6] Texas Instruments,TMS320x2833x,2823x System Control and Interrupts Reference Guide,2010.