High-k Gate Stacks Influence on Characteristics of Nano-scale MOSFET Structures

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***Abstract*—The models of electro-physical effects built-into Sentaurus TCAD have been tested. The models providing an adequate modeling of deep submicron high-k MOSFETs have been selected. The gate and drain leakage currents for 45 nm MOSFET with PolySi gate and SiO_2, SiO_2/HfO_2 and HfO_2 gate dielectrics have been calculated using TCAD. It has been shown that the replacement of traditional SiO_2 by an equivalent HfO_2 dielectric considerably reduces the gate leakage current by several orders due to elimination of the tunneling effect influence. Besides, the threshold voltage, saturation drain current, mobility, transconductance, etc. degrade within 10-20% range.**

Keywords-component: MOSFET; high-k materials; TCAD; physical models.

I. INTRODUCTION

In novel microprocessors produces by Intel, AMD, Apple, Samsung, NEC Electronics high-k gate CMOS devices are used. In recent years high-k gate nano-scale MOSFETs became to real candidates to reduce standby power consumption of CMOS VLSIs due to their possibility in reduction of gate leakage current in comparison with conventional silicon dioxide gate structures. In previous works the electro-physical behavior of unirradiated high-k gate MOSFETs using Sentaurus [1]-[4] and ATLAS [5], [6] device modeling tools was analyzed. However, the use of high-k gate dielectric also effects the rest characteristics of MOSFETs which need to be studied in detail.

In our work according to the modeling and design strategy for nanoelectronics devices supported by European Nanoelectronics Initiative Advisory Council we have realized the TCAD modeling procedure to achieve close match between TCAD modeling results and experimental characteristics.

II. PHYSICAL TCAD MODELS

All the physical models of mobility, scattering, carrier transport, tunneling, quantization, generation–recombination, hot-carrier injection implemented in Sentaurus version J-2014.09 were examined. The set of adequate models was selected and recommended for high-k gate MOSFET design (see Table I).

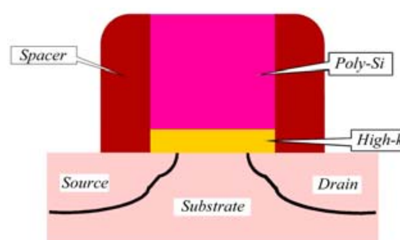

Figure 1. MOSFET structure withhigh-k gate insulator.

TABLE I. SET OF TCAD PHYSICAL MODELS FOR HIGH-K SIMULATION

Models	Gate Oxide		
	SiO_2	*SiO_2/HfO_2*	*HfO_2*
Transport Model	Hydrodynamic		
Carrier–Carrier Scattering	CarrierCarrierScattering(BrooksHerring)		
Mobility Degradation	Enormal		Enormal (Lombardi_highk)
Generation–Recombination	SRH(DopingDep), Auger		
Quantization	Density Gradient Quantization Model		
Tunneling	DirectTunneling		
Hot-Carrier Injection	Lucky		

The experimental works [7]-[16]where the main physical parameters describing the silicon-dioxide surface discrete trapped charges; device doping profiles; electron and hole mobilities of conversional and SOI FETs with different gate stack and others were analyzed. The real input data for the physical parameters used in Sentaurus tool for different high-k gate FET structures simulation were established.

In [6]-[8] have shown that the carriers capture more intense at HfO_2/Si interface than at SiO_2/Si interface. The values of the surface states charge (Q_{int}) for SiO_2, HfO_2 and SiO_2/HfO_2 dielectrics assumed to be $5 \cdot 10^{10}$, $5 \cdot 10^{11}$ and $1 \cdot 10^{12}$ cm^{-2} respectively. Similar Q_{int} values are used in [5] and [6].

Direct Tunneling model parameters were modified with using [9].

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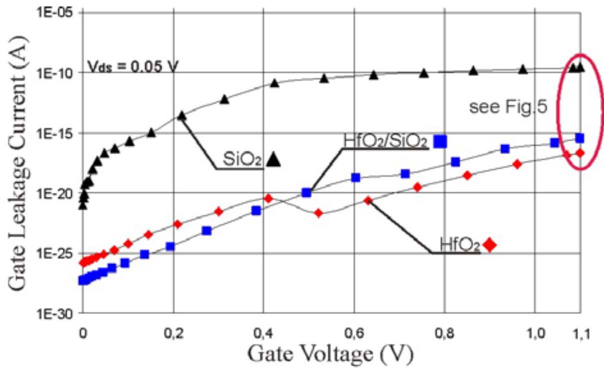

Figure 2. Gate leakage current for high-k MOSFETs with different gate oxide.

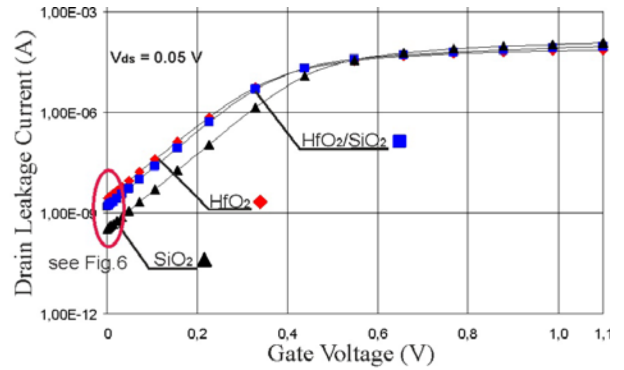

Figure 4. Id-Vg characteristics for high-k MOSFETs with different gate oxide.

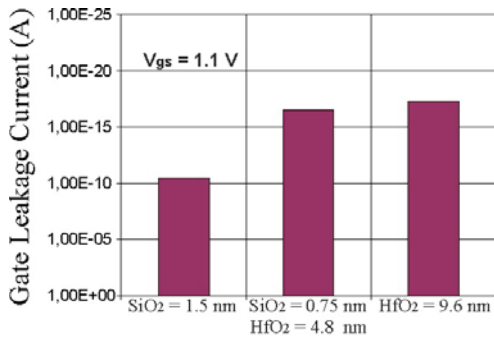

Figure 3. Comparison of Gate leakage current for high-k MOSFETs with different gate oxide.

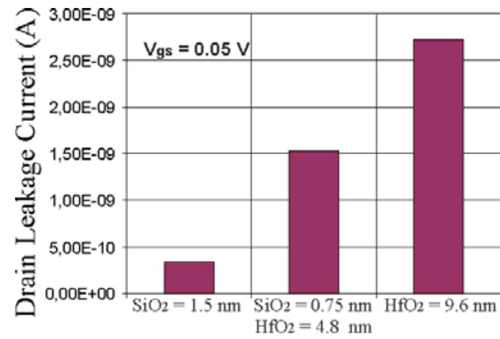

Figure 5. Comparison of Drain leakage current for high-k MOSFETs with different gate oxide.

III. 45NM MOSFET MODELING

The calibration of electrical characteristics for different high-k gate MOSFETs was carried out comparing I-V characteristics obtained from TCAD simulations and those from measurements.

45nm MOSFET structure with polysilicon gate (W_{poly} = 500 nm, L_{poly} = 45nm) was simulated. Different gate dielectric: SiO_2, HfO_2 and composite (stack) of SiO_2 and HfO_2 were used. For all modeled MOSFET structures EOT was set at 1.5 nm (see. Fig.1).

$$EOT = t_{high-k} \cdot \left(\frac{k_{SiO2}}{k_{high-k}}\right).$$

The doping of the silicon source/drain region is assumed to be $1 \cdot 10^{20}$ cm^{-3}. The peak value of doping concentration in silicon channel region is assumed to be $1 \cdot 10^{18}$ cm^{-3}.

The doping concentration in polysilicon gate is $1 \cdot 10^{22}$ cm^{-3} at the top and $1 \cdot 10^{20}$ cm^{-3} at bottom of the polysilicon gate.

Threshold voltage (V_{th}), drain leakage current (I_{off}) and gate leakage current (I_{gate}) were calculated at a lower voltage (V_{ds}=0.1 V, V_{gs} from 0 to 1.0 V). Saturation drain current (I_{on}), mobility (μ) and transconductance (S) were calculated at a high voltage (V_{ds}=1.0 V, V_{gs} from 0 to 1.0 V). The values of the basic parameters for 45nm MOSFET with the three types of gate dielectric are collected in Table II.

TABLE II. PARAMETERS OF 45NM HIGH-K MOSFET WITH DIFFERENT GATE OXIDE

Parameters	Gate Oxide		
	SiO_2 1.5 nm	*SiO_2 0.75 nm / HfO_2 4.8 nm*	*HfO_2 9.6 nm*
I_{gate}, A	2.82E-10	3.26E-16	2.10E-17
V_{th}, V	0.42	0.38	0.37
I_{off}, A	3.35E-10	1.53E-09	2.72E-09
I_{on}, mA	1.12	1.0	0.84
μ, m/(V·s)	168	133	125
S, uA/V	330	290	210

Table II and Fig. 2 and Fig. 3 show that the gate carrier tunneling effect could be pressed and gate leakage current could be considerably 6-7 orders reduced by replacement traditional SiO_2 gate dielectric of equivalent HfO_2 dielectric.

The rest of important MOSFET parameters: threshold voltage, saturation drain current, mobility, transconductance etc. degrade after replacing SiO_2 with HfO_2 in MOSFETs with polysilicon gate (see Fig.3-Fig.6).

The presented TCAD simulation results agree with experimental I-V characteristics investigations [1], [4] and [13].

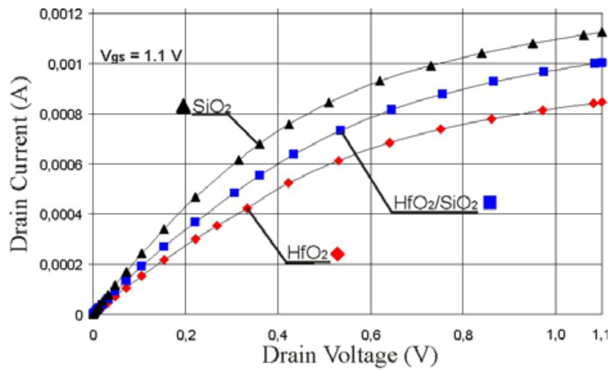

Figure 6. Id-Vd characteristics for high-k MOSFETs with different gate oxide.

IV. CONCLUSION

The physical TCAD models providing an adequate modeling of deep submicron high-k MOSFETs have been selected. I-V characteristics of 45 nm high-k gate MOSFET on bulk substrate were simulation with selected models for confirm their adequacy.

ACKNOWLEDGMENT

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