A 12 Bit IF Sampling Pipelined ADC in 0.18um BiCMOS

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Abstract. In this paper, a 12 bit 500MS/s IF Sampling ADC is described. The ADC has an integrated input buffer with a new linearization technique that improves its distortion. Eight pipeline stages with fully differential switched capacitor architecture follow the input buffer. Each of stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier(MDAC). A 0.18μm BiCMOS process with 1.8V analog power supply is used in the design. This ADC achieves an SNR of 65dB and an SFDR of 82dB for sampling analog input frequencies up to 250MHz

Introduction

Many communication and signal processing system are demanding >60dB dynamic range while sampling intermediate frequencies that may range from 100MHz to 500MHz. This paper describes a 12-bit 500MS/s ADC with high linearity input buffer. Section 2 gives a detailed overview of the architecture and describes all key building blocks. Section 3 gives a detailed circuit description of the input buffer、pipelined ADC stages、residue amplifier. Section 4 gives experimental results of the ADC.

Architecture Overview

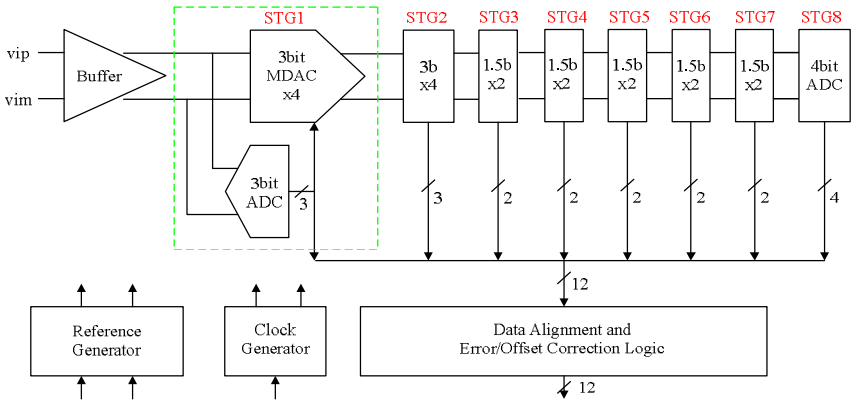

Fig. 1 12-bit ADC architecture

A block diagram of the 12-bit ADC architecture is shown in Fig.1. This SHA-less ADC consists of a differential input buffer followed by eight pipeline stages. The differential input buffer accepts a 1.5Vp-p differential signal. Following the input buffer is a 3-bit MDAC with 1 bit of redundancy to improve comparator offset tolerance. The 3-bit MDAC is followed by another 3-bit MDAC with 1 bit of redundancy and 5 1.5b/stages. The final 4 lsb's are converted by the backend 4 bit flash converter. Each stage of the pipeline consists of sub ADC、DAC and residue amplifier. The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

This ADC also includes reference and clock generator. A differential voltage reference creates positive and negative reference voltages that define the 1.5Vp-p fixed span of the ADC core. A clock

circuit based on dynamic delay line (DLL) provides all kinds of phases clock to every part of the pipelined ADC.

Key Building Blocks

Input Buffer Circuit

Today the high-speed and high-resolution ADC often adopts SHA-less architecture to reduce power, which requires a input buffer with wide bandwidth and high linearity. Also, Adding an input buffer at the ADC front end has the advantage of isolating ADC sampling glitch of the switched capacitor circuit from affecting the external ADC driver circuit. A broadband buffer is relatively easy to implement with emitter follower in a BiCMOS process as high speed NPN devices are available.

High linearity input buffer should have high input impedance and low output impedance, High input impedance can isolate input driver circuit from noise interference produced by sampling switch. Low output impedance can decrease distortion produced by nonlinear load impedance.

This paper proposes a input buffer which can decrease relativity between the g_m of input transistor and input siginal, makes the g_m of input transistor invariable to input siginal, even keeps a constant. It is well known that the g_m of input transistor is decided by its bias current, the bias current of input transistor keeps invariable, so that the g_m of input transistor keeps invariable. Figure 2 is the input buffer with repilca load impedance proposed by this paper. It includes a input transistor NPN Q1, a load capacitor C_L, a replica load capacitor C_{RL}, a constant current source I constituted by a NPN Q2 and a NMOS M2.

Adopting the input buffer with replica load impedance proposed by this paper, the AC small siginal current i_L following input siginal variety on the load capacitor can be provided by siginal source via replica load capacitor. This guarantees that the bias current of input transistor NPN Q1 keeps invariable, so that the g_m of input transistor NPN Q1 keeps invariable and output siginal distortion will be decreased.

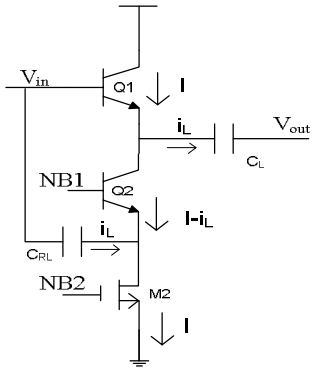

Fig.2 Input buffer with replica load impedance

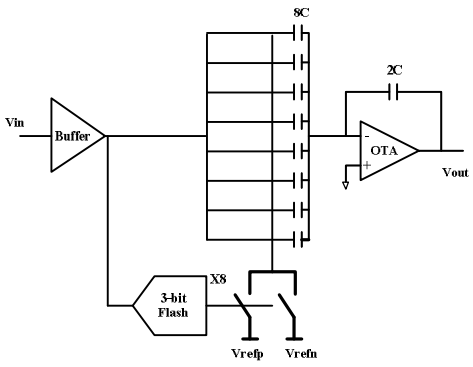

Fig.3 1st stage pipeline architecture

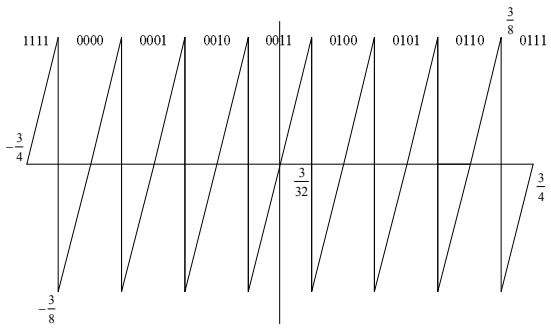

Fig.4 1st stage output residue curve

Pipelined ADC Stages

This ADC have a SHA-less analog front end. Followed the low distortion input buffer, a 3bit architecture is chosen for the ADC's 1st stage. One bit redundancy is added to increase the sub-ADC

comparator offset tolerance. Multi-bit/stage architecture has been widely used in high speed and high resolution pipelined ADC designs, especially in ADC's front end stages. It has the advantage of reducing the capacitor matching requirement, improve ADC linearity. Fig.3 shows the 1st stage pipeline architecture.

The 1st stage flash ADC has sampling networks for its comparators that closely match that of the MDAC. This is needed because any mismatch in the comparators causes the input value sampled by the MDAC to be different from that sampled by the comparators. This leads to flash offset and gain errors that get worse with increasing the input frequency. This error consumes a portion of the correction range of the first stage residue ,but can be corrected by the digital error correction only as long as the residue does not exceed the correction range. During the sampling phase, the input is sampled on the MDAC and the flash sampling capacitances. During the hold phase, the flash comparators make their decisions and propagate them to the DAC switches, which connect the DAC capacitances to either Vrefp or Vrefn depending on the flash bits. Fig.4 shows the 1st stage output residue curve.

The ADC's 2nd pipeline stage is also a 3bit stage with 1bit redundancy. 8 comparators are used in its sub-ADC. According to pipelined ADC theory, the 2nd pipeline stage circuit requirement is relaxed by the gain of the 1st pipeline stage. Although the architecture of the 2nd pipeline stage is same to the 1st pipeline stage, the size of sampling capacitances and switches becomes smaller, the adoption of residue amplifier is different and power consumption decreases.

1.5b/stage architecture is used in stage 3~7. As errors introduced in stage 3 are attenuated by the front stage gain of 16, the noise and matching requirement in these stages are greatly relaxed. Only 8bit matching accuracy is required for 3rd stage MDAC, even less is needed for later stages. So MDAC capacitors can be scaled down to improve the circuit speed, and reduce ADC power consumption. Fig.5 shows the 1.5b/stage architecture. Fig.6 shows its output residue curve.

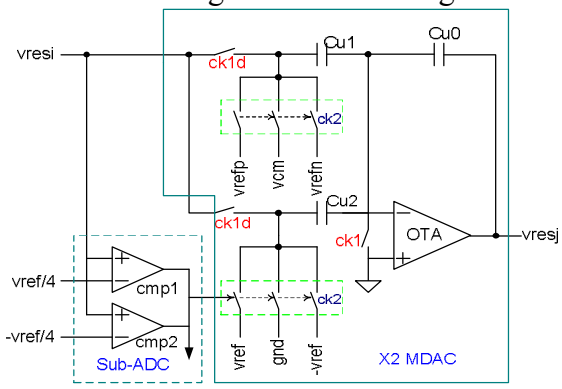

Fig.5 1.5b/stage architecture

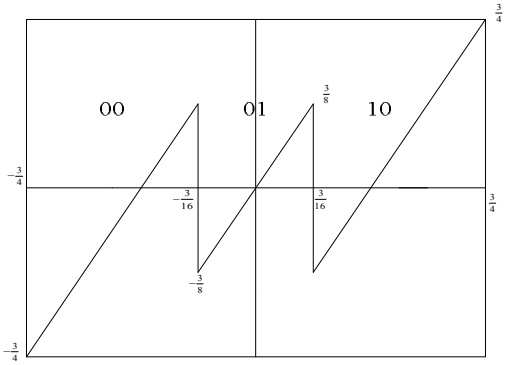

Fig.6 1.5b/stage output residue curve

The last stage is simply a 4bit flash ADC, as no residue voltage needs to be generated for further processing, so the MDAC is removed. 14 comparators are used in the last stage and its outputs are coded from 0000 to 1111.

Residuse Amplifier Design

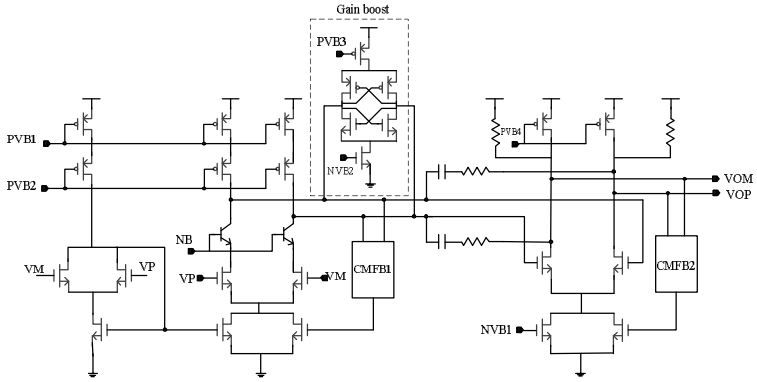

Fig.7 1st stage pipeline residue amplifier

The 1st stage pipeline residue amplifier is shown in Fig.7 and consists of two stages. The first stage is a cascoded amplifier with double-cascoded PMOS and BJT-cascoded NMOS. The first stage has also a gain boost block. This circuit uses positive feedback, through cross-coupling, to create a negative trans-conductance circuit in parallel with the main devices. The second stage is a simple differential pair with PMOS current source and resistor load. The Miller compensation capacitances are connected between the outputs of the second stage and the outputs of the first stage. The first stage and the second stage have each a common mode feedback (CMFB) block. The bandwidth required for the 1st stage pipeline residue amplifier to achieve 12-bit performance is about 1.2GHz and the open loop gain needs to be larger than 80dB. This required high gain-bandwidth product leads to high power consumption in 1st stage pipeline.

The 2nd stage pipeline residue amplifier architecture is different to the 1st stage pipeline residue amplifier. Because the requirement of 2nd stage pipeline residue amplifier is relaxed, the BJT NPN is no more needed. It is replaced by NMOS. The residue amplifier architecture in stage 3~7 is same to the 2nd stage pipeline residue amplifier. But their sizes and power consumption are scaling down along with pipeline stages according to pipelined ADC theory.

Experimental Results

The 12bit ADC is fabricated on a 0.18μm BiCMOS process. Fig.8 shows an FFT Spectrum of a 30.3MHz sinewave sampled at 500MSPS. SNR is 65.6dB and SFDR is 82.1dB. Fig.9 shows DNL and INL of this ADC. The 12bit ADC performance is summaried in the following table.

Table 1 This ADC performance summary

Technology	0.18μm BiCMOS
Supply Voltage	1.8[V]
Differential Input Range	1.5[Vp-p]
DNL/ INL	±0.4[LSB]/±0.9[LSB]
SNR/SFDR	65.6[dB]/82.1[dB]
Power Dissipation	700[mW]

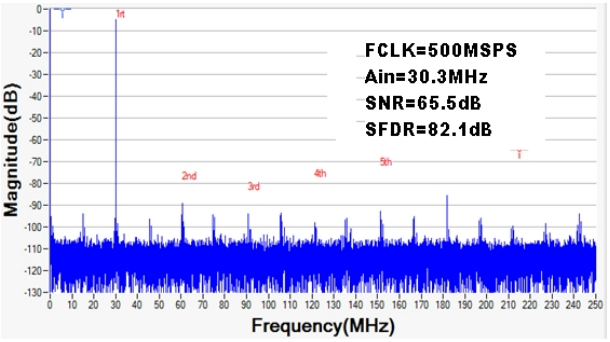

Fig.8 FFT Spectrum

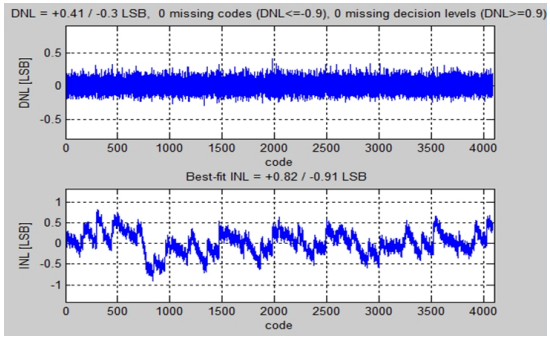

Fig.9 DNL and INL

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