A 14-b 500 MSPS Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration

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Abstract. This paper presents a 14-bit 500MSPS ADC in 0.18 um CMOS process. By interleaving two 250MSPS ADCs, a sample rate of 500MSPS is achieved. The offset, gain error and time skew between the two channels are calibrated in the background. The measurement shows that the ADC has performances of 10.6 bits ENOB, 78dBc SFDR, 4 by 4 square micrometers area and 950mW power consumption under power supply of 1.8V.

Introduction

As the need for higher signal bandwidths increases, the requirement for ADCs with higher sampling rates grows correspondingly. Applications such as software radios, power amplifiers, linear data acquisition and test equipments all need higher bandwidths and accuracy.

The most promising topology for a high-resolution, high-speed A/D converter implemented in a CMOS process is the pipeline architecture. Parallel pipeline ADCs with several time interleaved component ADCs have been introduced to attain very high sampling rates with acceptable power consumption. However, analog parallelism suffers from path mismatch errors, limiting the potential performance gain attainable through interleaving. Digital calibration techniques have been widely reported in the past to mitigate the mismatch errors in TI-ADC arrays [1] [2]。As the resolution and speed of ADCs used in time-interleaved ADCs increases, the demands on clock, offset, and gain match become more and more tough. Because of that, 14-bit or higher resolution time-interleaved ADCs are rarely reported.

In this paper, a 14-bit 500MSPS ADC is realized through time-interleaving two 14-bit 250MSPS ADC. The offset, gain error and time skew between the two channels are calibrated in the background. The proposed 14-bit 500MSPS ADC is implemented in a 0.18um CMOS process. The measurement shows that the ADC has performances of 10.6 bits ENOB, 78dBc SFDR, 4 by 4 square micrometers area and 950mW power consumption under power supply of 1.8V.

The structure of the proposed time-interleaved ADC

Shown in figure 1 is the structure of the proposed 14-bit 500MSPS time-interleaved ADC, where two 14-bit 250MSPS ADCs are running in parallel. The analog signal X(t) is put into the two ADCs through a clock-controlling block. The offset and gain error between the two ADCs are calibrated through a digital calibration cell. The time skew between the two channels is calibrated through the adjustable delay-lines, which is controlled by the digital calibration cell. The final data are output by a MUX cell.

Shown in figure 2 is the structure of one channel 14-bit ADC applied in figure 1. The 14-bit ADC includes several pipelined stages, a reference circuit, a clock-stabling circuit, a logical control circuit, a digital correction circuit and an interface circuit. The first pipelined stage includes a 4-bit flash ADC, with the second pipelined stage including a 3-bit flash ADC, the 3-8th pipelined stages including a 1.5-bit flash and the last pipelined stage including a 3-bit flash ADC.

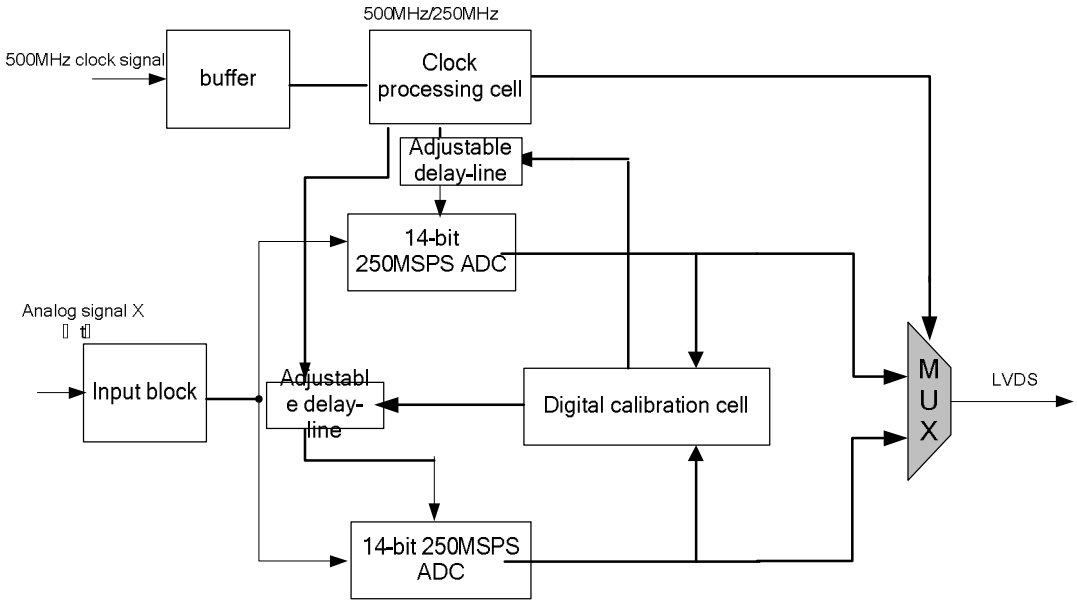

Figure 1. The structure of the 14-bit 500MSPS time-interleaved ADC

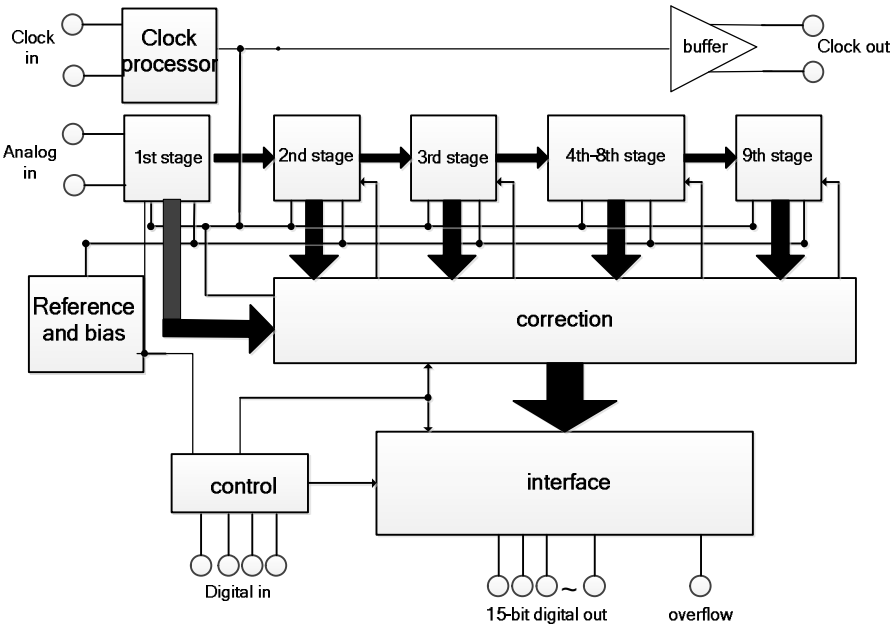

Figure 2. The structure of one channel 14-bit ADC

The 14-bit ADC shown in figure 2 doesn't have a sampling and holding circuit in the front. The sampling and holding function in built in both Flash ADC and MDAC of the first stage. The front part of the 14-bit ADC without sampling and holding circuit is shown in figure 3. The advantage of such architecture is that the sampling and holding amplifier is omitted, resulting in lower power consumption, noise figure and distortion.

Calibrate the mismatches between the two channels in time-interleaved ADC

Time interleaving techniques can double or multiply by N the sampling rate of ADCs. Though, the mismatches between interleaved channels will degenerate the performances. In this paper, the offset, gain error and time skew are calibrated in the background through a way which includes both analog and digital processing. The offset, gain error and clock skew are estimated using an adaptable signal processing technique. Then, the offset and gain error are calibrated through a pure digital way. A digital-analog feedback loop is formed to calibrate the errors caused by the clock networks through

ways of digital control of adjustable delay line. A pure digital feedback loop is formed to calibrate the offset and gain error among channels. Consequently, the system is less complicated to implement with considerable flexibility. Also, the power consumption is cut down.

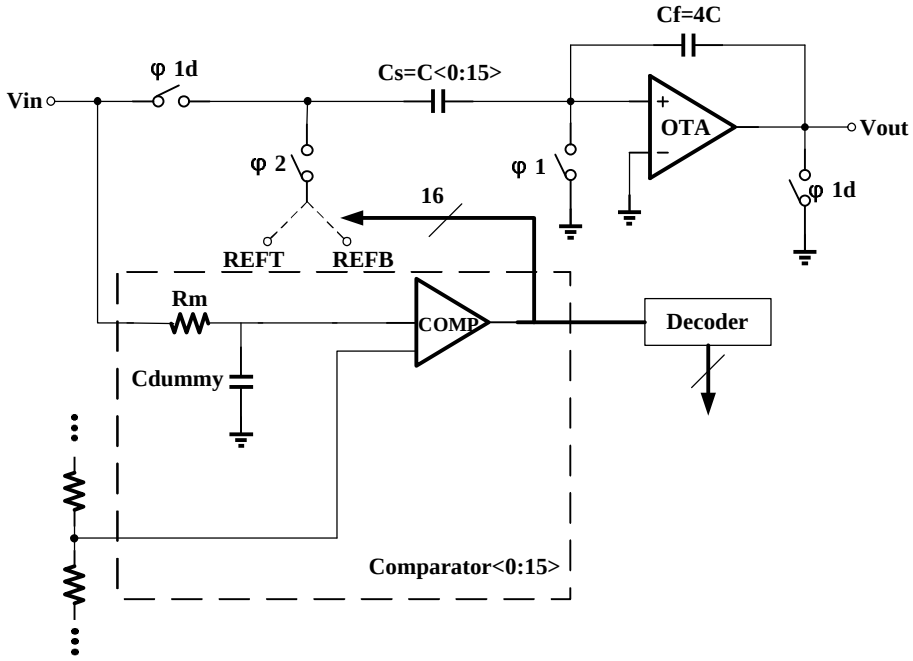

Figure 3. The analog front part without a sampling and holding circuit

The clock skew between channels is calibarted through ways of digital-analog mixed processing. During the calibration, the adjustable delay line lies in the feedback look of mixed-signal circuits. Since the adjustable delay line is placed directly in the clock path, its design is crucial as ADC dynamic performance is a function of the sampling edge jitter.

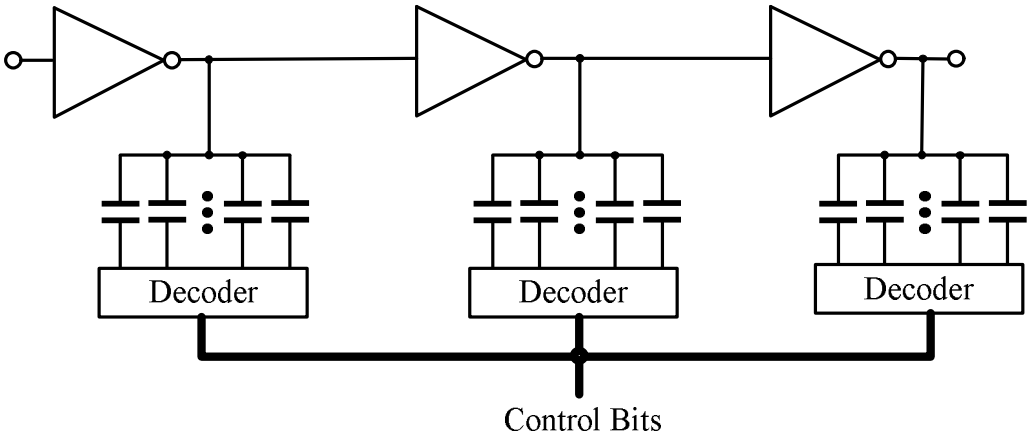

Figure 4. Time-delay cell

If only one inverter is used in the adjustabe delya cell, the rising or falling edge will be very slow, wich will degnerate the dynamic performances. In order to sovle such problem, serval inverters are used in the delay line as shown in figure 4. The controll codes are the combination of binary and thermometer codes. Because metal capacitors are precise and linear, they are used in the adjustable delay line. The total simulated correction range was 20ps with a step size of approximately 50fs。

Measurement results

The 14-bit 500MSPS ADC is taped out in a 0.18um CMOS. The measurements show that the INL is 1.5LSB, and the DNL is 0.7LSB, as shown in figure 5; the ENOB is 10.6 bits, the SNR is 66dB and

the SFDR is 78dB，as shown in figure 6. The areae of the chip is 4 by 4 micrometers, consuming only 950mW under 1.8V power supply.

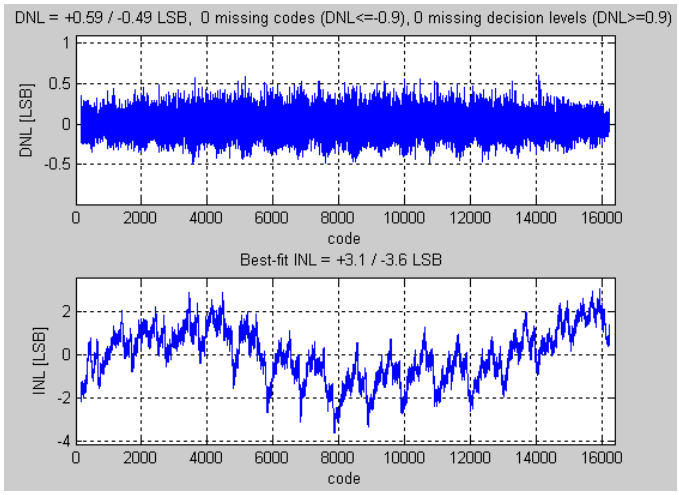

Figure 5. The static performances of the proposed 14-bit 500MSPS ADC

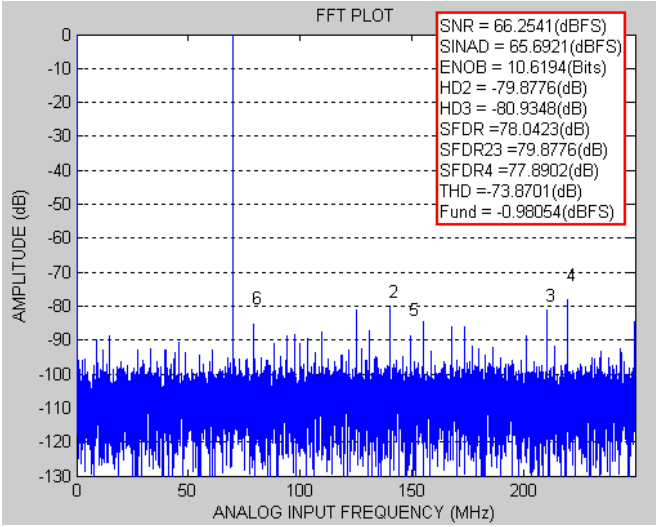

Figure 6. The dynamic performances of the proposed 14-bit 500MSPS ADC

Summary

In this paper, A 14-bit 500MSPS ADC is realized through time interleaving two 14-bit 250MSPS ADCs. In order to fulfill 14 bit resolution, an adaptable estimation algorithm is applied to background calibrate offset, gain error and clock skew between channels timely.

References

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