# Design and Implementation of a High Efficient DDR SDRAM Controller Applied in TOF-MS

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**Abstract.** Owing to large capacity and high speed, DDR SDRAM has been widely used in the data acquisition system of time-of-flight mass spectrometer (TOF-MS) which can detect and analyze biological and chemical macromolecule precisely. Due to the particularity of the requirement of large amounts of data accumulation in TOF-MS signal processing, the time cannot be efficiently used during reading and writing in traditional design of DDR SDRAM controller. This paper presents a new strategy of reading and writing, increasing the efficiency of data processing greatly and finally a DDR SDRAM controller has been implemented. Software simulation and hardware implementation prove the correctness and feasibility of this design and the efficiency of reading and writing reach up to 93.6%.

## Introduction

In the time-of-flight mass spectrometer (TOF-MS), how to collect and process the data quickly and accurately is a key issue [1]. High speed data acquisition has characteristics of high data throughput and requires transmitting and storing the data stream in short time. But the on-chip memory space of FPGA is too small to meet the large quantity of data generated by TOF-MS. So it is necessary to design extra memory. DDR SDRAM transfers data on both edges of every clock cycle, effectively doubling the data throughput of memory device. And it has been used widely on PC for its low cost [2, 3]. So DDR SDRAM is applied as the memory device of high speed data acquisition in this paper.

Although DDR SDRAM has the advantage of high speed and large capacity, various time latencies decrease the data transmission efficiency of DDR SDRAM greatly. Many researches have been undertaken in this field. Design of DDR Controller for satellite navigation receiver was proposed in[4]. An SDRAM controller for video signal processing was designed in[5, 6]. Some DDR controllers designed for general conditions were showed in[7]. But all of these designs are not fit for the data acquisition of TOF-MS because there is a need to accumulate 5~6 times of sample signals together in order to reduce the signal to noise ratio (SNR). So we propose an SDRAM controller applied in TOF-MS with high efficiency of data transition in this paper.

## Principles of DDR SDRAM Controller Design

**Brief introduction of high speed data acquisition system.** Fig. 1 shows the structure of high speed data acquisition board of TOF-MS. The input signal is interleaved sampled by the two analog to digital converters integrated in one ADC07D1520 chip which can get a maximum sample rate of 3GSPS and a output bit width of 32 bits, as described in[8]. System control including DDR control is realized by XC7K325TFFG676 of Xilinx Kintex-7 family. In this design, MT41J64M16, one of DDR3 series with the features of high clock frequency, low power consumption and low cost is implemented as memory chip. The memory depth of this chip is 1Gb. It consists of 8 banks and each bank has 4096 rows while each row has 2KB capacity. The data width is 16 bits and two chips are used in parallel to extend data width to 32 bits.

 

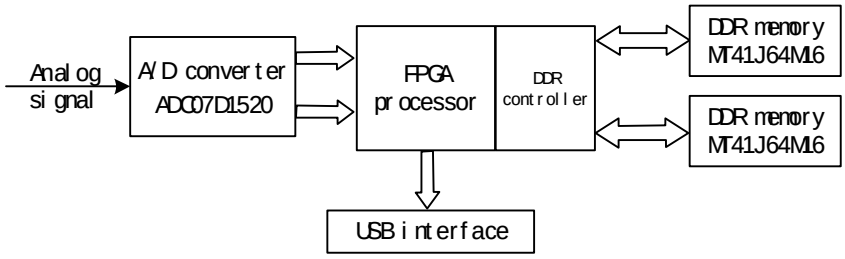


Figure 1. Structure of high speed data acquisition board of TOF-MS

**Principles of increasing efficiency.** The bandwidth usage efficiency is the ratio of valid write/read time and total time used in write/read operation [9, 10]. For example, a write operation includes active, write and precharge commands etc. and data writing which is valid time is completed only during write command. Those control commands and many time latency parameters generated by the limitation of semiconductor technology are main factors to reduce the efficiency of DDR memory.

MT41J64M16 provides a series of commands controlled by some mode registers. Some major commands are listed in Table 1.

Table 1 . Major commands of MT41J64M16

| Command | CS# | RAS# | CAS# | WE# | Function |
|---|---|---|---|---|---|
| ACTIVATE | L | L | H | H | Open a row in a particular bank |
| READ | L | H | L | H | Initiate a burst read access to an active row |
| WRITE | L | H | L | L | Same as READ |
| PRECHARGE | L | L | H | L | Deactivate the open row in a particular bank |
| REFRESH | L | L | L | H | Guarantee stored data valid |

A memory-access operation consist of three steps. First, an ACTIVATE command is used to open a row in a particular bank for a subsequent access. Second, a burst-length command along with READ/WRITE is issued to initiate a burst length data access to the active row. Finally, when a row of a bank is finished, another row should be open. But changing rows in DDR SDRAM means a PRECHARGE command to close the current row and then an ACTIVE command to open a new row for a subsequent access. After completing these, the address is accessible for the READ or WRITE command. Then the delay of two read/write access is the total of tRP (precharge time), tRCD (active time) and CL (CAS latency), which significantly reduces the efficiency of reading and writing. These invalid time are called overhead cycles.

These overhead cycles can't be eliminated but can be overlapped. One method is to read or write data into the same row continuously. In this condition, other columns on the same row can be accessed by changing only the column address without invoking any additional row close and activation, avoiding time consumption of ACTIVE and PRECHARGE commands. Another method is multi-bank interleaved accessed. When a row access has been finished, the subsequence data must be put into different banks so as to hide inevitable overhead cycles generated by the activation and precharge commands when changing rows. Note that send ACTIVE command to the new row prior to the finish of the former row in order to realize that access data seamless. To avoid data interference, write command can't follow read command without latency neither in the same bank nor in different banks. So we must separate read and write as much as possible.

## Implementation of DDR SDRAM Controller

DDR SDRAM controller controls the access to memory in accordance with the timing rules, including a arbiter, state controller of 8 banks, command controller, I/O controller, etc. The controller initializes DDR memory, parses the issued commands from user, and generates all the control signals required for the memory and the user interface. The logic block diagram is shown in Fig. 2

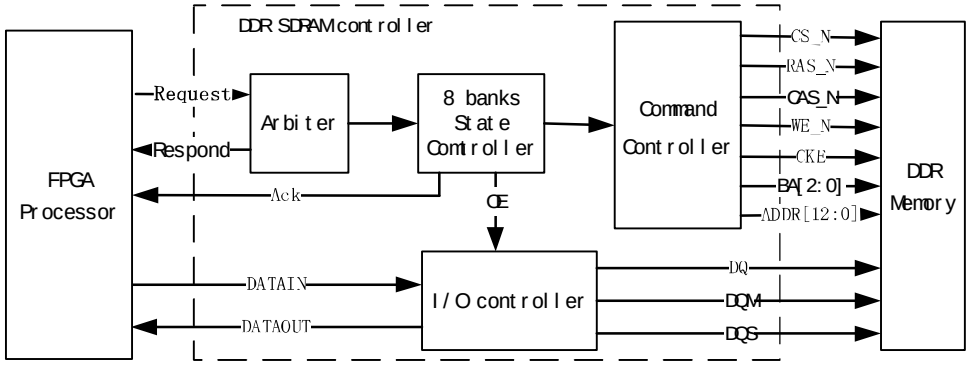


Figure 2 Logic block diagram of DDR SDRAM controller

Fig. 3shows banks interleaved accessed state machine of DDR controller. Previous to read or write operation, DDR SDRAMs must be powered up, initialized and calibrated in a predefined manner. When these operations are done, the controller comes into idel state, which indicates the start of normal operation. Then the controller can start issuing user write and read commands to the memory.

In the design of controller, Read and write accesses to the DDR SDRAM are burst-oriented. The burst length determines the maximum number of column locations accessed for a given READ or WRITE command, and the value can be programmable to either 4 or 8. In this design, the burst length is set to be 8 to make data access continuously, increasing the efficiency of read and write.

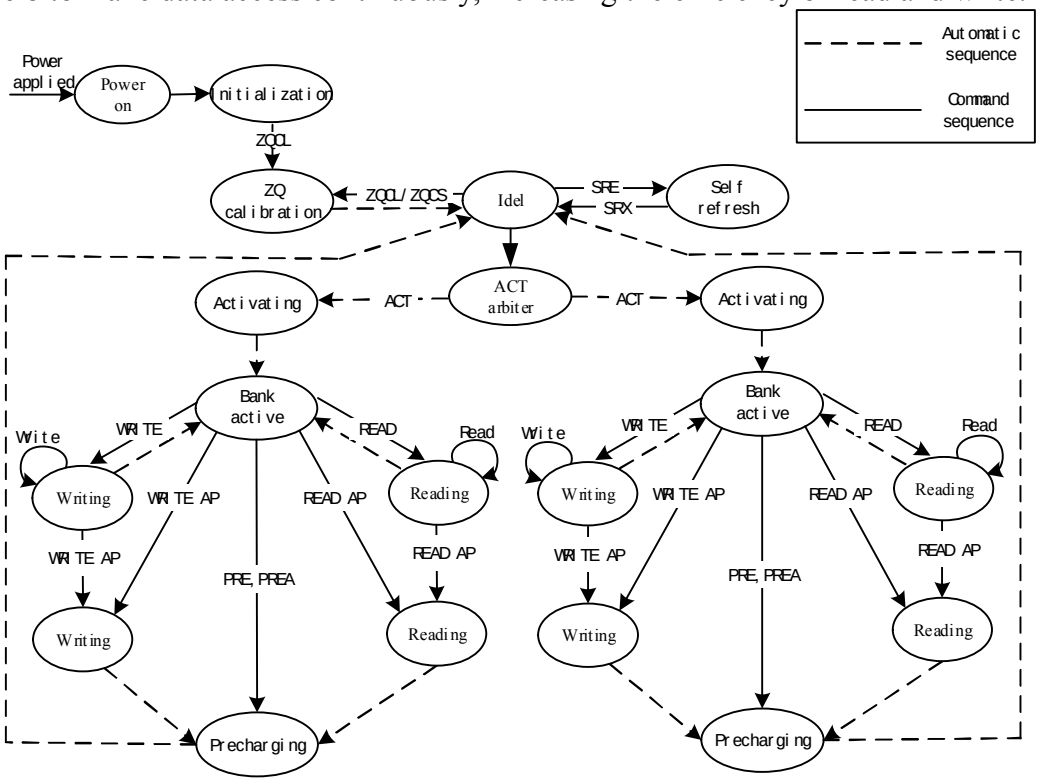


Figure 3 Banks interleaved state machine of DDR controller

## Functional Simulation and Analysis

DDR SDRAM memory has complex and rigorous control logic and timing requirements, but the DDR SDRAM controller provides a relatively simple user interface. This paper conducts functional simulation as the aforementioned algorithm by Verilog in Xilinx Vivado 14.4 IP cores to implement the DDR SDRAM controller. The simulation result shown in Fig. 5 indicates that the DDR SDRAM controller can work properly. The consecutive memory access makes the accessing data signal in ddr3_sram_a_dq continuous, thus increasing the data accessing efficiency greatly. We completed ten simulations and each simulation executed for one second. The average access efficiency is approximately 93.6%.

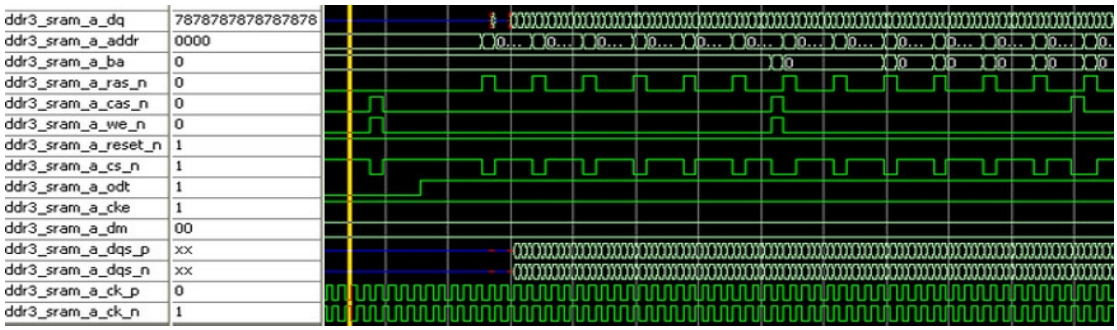

Figure 4 Simulation result of W/R

## Conclusion

In this paper, a high efficiency DDR SDRAM controller applied in 3GSPS high speed data acquisition board in TOF-MS is presented. Based on fully understanding of the principles of DDR SDRAM, an efficient overhead-reduce strategy is proposed for data access. The hardware system is implemented based on FPGA and the software design is completed according to the state transition diagram. The simulation results indicates that the design can not only work normally but also work efficiently.

## Acknowledgements

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