Hardware-configuration based on FPGA for open CNC system

SHUANQIANG Yang[12, a *],XINLONG Huang[2,b]

[1] College of Mechanical Engineering and Automation, Fuzhou University, Fuzhou,350108,China

[2]School of Engineering, Fujian Jiangxia University, Fuzhou, 350108, China

[a]yangshuanqiang@163.coml, [b] hxl881116@163.com,

Keywords: Open CNC system, FPGA, Hardware-configuration.

Abstract. In this paper, according to analyzing the domestic and foreign recent research status and future developments of open architecture CNC system, an open soft system with configurable architecture based on PC + programmable I/O interface card has been studied. The research is studied for the drawbacks of existing open CNC system based on PC and the unresolved problems of preliminary study presented by the research group, to satisfy the development requirements of low cost, high performance that means high speed, high precision and the large amount of data processing, configurable architecture and modularization. Meanwhile, this dissertation makes systematic and deep going study on function requirements, structure planning based on programmable I/O interface card, hardware-configurable modeling, circuits design of control chip, task assigning between software and hardware and servo control.

Introduction

Open Computer numerically controlled (CNC) is implemented to configure system including software-reconfiguration and hardware-reconfiguration, as to widely be used in different working conditions. Software-reconfiguration is generally based on motion control card, such as the PMAC motion controller, which is integrated with cutter compensation, interpolation algorithm and position control. Reconfiguration of system is just achieved by independently programming on the software layer; hardware-reconfiguration is made full use of the reconfiguration of programmable logic device to build control core of CNC and realize CNC system configuration by hardware description language (HDL). In this regard, there have been a lot of researches.

Koren [1] mainly through modular system design scheme for a variety of processing equipment system combination, meet the demand of different types of products. According to different the type of tasks and hardware devices, Bi [2] reconstruct the manufacturing systems by configuring the combination of different hardware devices to adjust the maximum degree of system capacity. Pritschow [3] has researched open controller, pointing out the open controller is to achieve reconfigurable manufacturing system key technologies. Padayachee [4] has proposed a modular reconfigurable CNC machine design method, by the method can achieve in a control platform for a variety of cutting operation and control degrees of freedom. Moon [5] design reconfigurable CNC machine tools, which meet the demand of the specific environment, by adopting space modeling, geometric structure and topological structure analysis, function mapping and control, equipment selection. S chreyer [6] used PLC to control the system through different subsystem modular, which can meet the needs of the different environment of CNC system.

These studies are able to reconstruct the numerical control system, but the reconstruction process varies. Someone is based on Multi-Agent [7]. Owing to be constituted by multiple FPGA, Multi-Agent is much Coordination and flexible but for large resources. The final configuration is realized through the call of software layer. The other research on reconfiguration is mainly committed to duplicate download on the hardware layer or the call program of software layer [8, 9]. However, this method is not high degree of flexibility.

In order to overcome these problems, new methodology is being developed for the reconfiguration of system based on PC + programmable I/O interface card. In this case, the real-time tasks are integrated into a single piece of FPGA, and hardware and software cooperative reconfiguration is

developed. Hardware- reconfiguration based on certain software- reconfiguration and its specific implementation is mainly introduced in this paper.

Structure of Hardware-configuration

Model of Hardware-configuration realization. Based on the architecture of PC + programmable I/O interface card and cycle data of a programmable I/O interface card are received from coarse interpolation operation by the PC, then the final fine interpolation is completed. In allusion to the problems of the Coarse and fine interpolation module transmission, the reference [10] proposed a data sampling interpolation method based on the offline course interpolation, using a dual caching mechanism and dynamic interpolation technology ensures continuity and reliability of interpolation. Fig.1 shows the structure of the asynchronous interpolation. On this basis, how to implement the reconstruction of the open CNC system and the hardware configurability with PC software layer will be the starting point of this study.

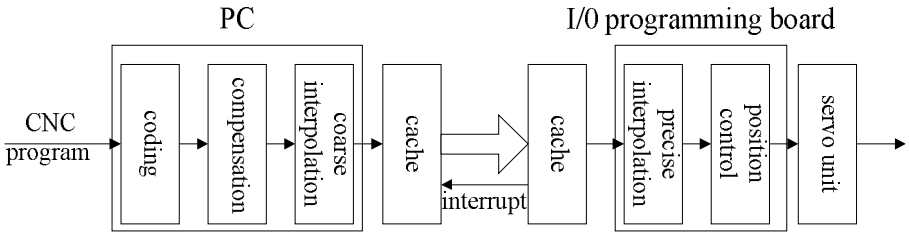

Fig.1. the structure of the asynchronous

Establishment of Model for Hardware-configuration.

Download of Configuration Information. The hardware configuration usually consists of static configuration and dynamic configuration. The former means that the system can be configured quickly by FPGA download and acquire the configuration information when the control system in the initial boot or system upgrade; the latter refers to the system can be partial configured quickly by the function module basis for different task downloads the configuration information, when the system is running.

Because of FPGA chip does not have the storage function of power off, the configuration information need to be re-download in each boot. Based on the This article is based on the idea of a static configuration, this paper proposes a method of PC online download configuration information, which means that the configuration information store on a PC, the configuration information need to be re-downloaded each boot (to ensure the software layer), and the configuration information need to be refigured only when the system upgrade. The advantage of this pathway is that the configuration information can be stored and refigured easily, the design of the hardware platform can be simplified, and the efficiency of the hardware card can be improved.

But it can only be determined to configuration before the system is running, as to the system is still in working condition, the method of configuration is likely to cause system instability.

Configuration Mechanism. Configuration data is written to a configuration module (CM) in programmable I/O interface card. A ready signal is built to prove the valid of configuration by setting high, which is generated from the command bits of configuration data. The data structure of command is shown in Table 1.

Tab.1. Data Structure of Command

2 Byte		2 Byte
Command code		Axis_enable code
bit15~bit12	bit11~bit0	
Group code	Group command code	
4H	000H	

Configuration signal is send to a data allocation module (DAM) when configuration data has been received and transformed. Meanwhile data transfer is controlled by the signal to open corresponding axis channel. The function of DAM is receiving the cycle interpolation data from FIFO module and the

data will be allocated according to the size of axis number and amount of axis. Hardware-reconfiguration structure is shown in Fig.2.

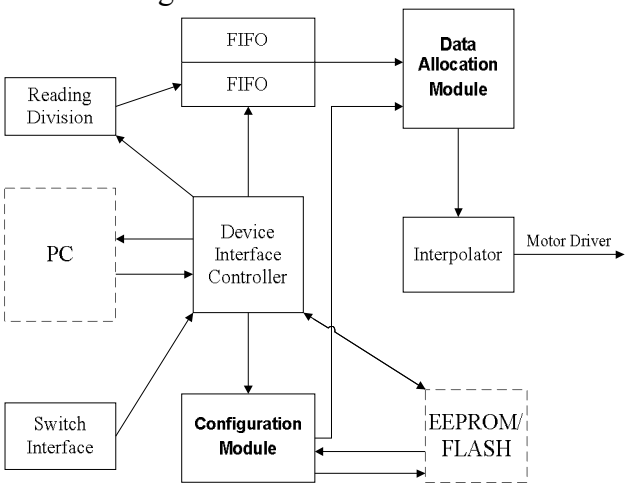

Fig.2.The diagram of hardware-configuration structure

Implementation and Testing of Configuration Circuit

The EP3C16Q240CN8 of Cyclone III device is selected as a main chip of programmable I/O interface card. According to owing high level of integration, low cost and design period of development and reconfiguration, the chip is ensured to be satisfied with the design of configuration circuit.

Configuration Module. Configuration module is applied to acceptance and transformation of configuration data as system boot. The configuration data that reflect the configuration demand for software layer is converted to a key enabling signal, which controls the flow of interpolation data as a gate signal.

Configuration module is divided into ready signal circuit and storage circuit. The component of ready signal circuit is four xor gates and one and gate. Command code is decoded in the ready signal circuit to generate ready signal. The implementation of storage circuit is achieved by a 2×32bit ROM setting 0 address to guarantee an unique Storage space; Axis enabling signal is send to next module when clock rising edge. The IP encapsulation for configuration module is shown in Fig.3. The timing simulation for configuration module shown in Fig.4 is demonstrated for an instance, that the low eight bits of configuration data ‘0x40000003’ is extracted to enable relevant axis, when signal ‘wren’ is valid. Meanwhile, Ready signal ‘crdy’ is put high to explain that configuration data is prepared.

Fig.3. IP Encapsulation for Configuration Module

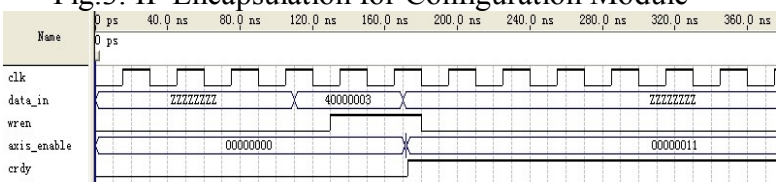

Fig.4. Timing Simulation for Configuration Module

Data Allocation Module. Data allocation module is applied to implement accurately logic allocation of rough interpolation read from FIFO according to configuration data. For instance, two words of 32-bits data are read from FIFO if enabling three-axes. Therefore, High 16-bits for the first

one of 32-bits data are reserved to ensure right distribution. The structure of collection datas is shown in Fig.5.

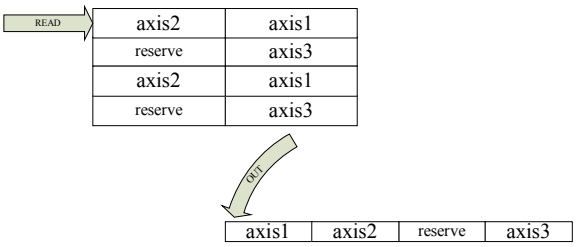

Fig.5. Communication Protocol of Interpolation

A register 'dinreg [127:0]' is set in data allocation module to meet configuration for eight-axes. Left shift and mnemonics for 32-bits number as each clock rising edge when written signal is valid. According to a generation of handshaking relationship between current module and upper module, signal 'wren' is same as written signal for upper module. Meanwhile, a D-flip flop is necessary for data keep because of clock delay and the signal after delay is called 'd_wren0'.

The IP encapsulation for data allocation module is shown in Fig.6. The timing simulation for data allocation module shown in Fig.7 is demonstrated for an instance, that data 'FFFX' for X-axis and data 'EEEE' for reserves will be sent to relevant output port 'outX' as clock rising edge.

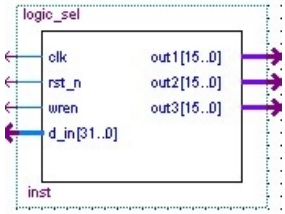

Fig.6. IP Encapsulation for Data Allocation Module

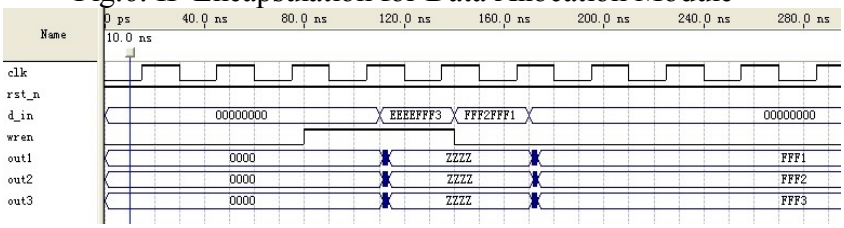

Fig.7. Timing Simulation for Data Allocation Module

Commissioning tests

In order to verify the design of the programmable device drivers for the I/O card and its function to meet the expected distribution and control requirements, in the study was carried out commissioning experiments. The experiment platform was shown in Fig.8. With three axes milling machine as the experiment platform of machine tool body, can control the X axis and Y axis and Z axis feed movement.

Fig.8. Commissioning test platform

The research group have completed software application development, and then for on-line testing, through the PC connected to the programmable I/O card, to connect to the 3 axis milling machine. The results shown in Fig9,Fig10.

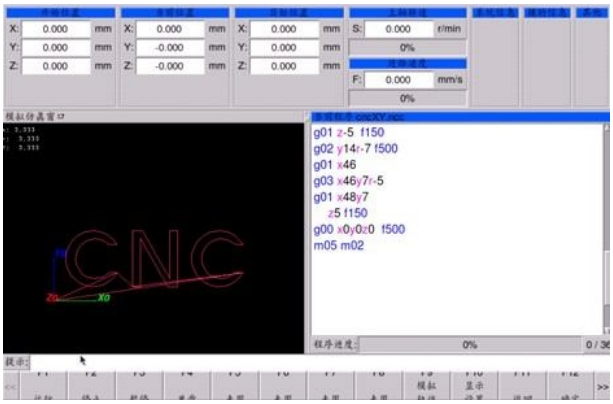

Fig.9 Simulated processing track

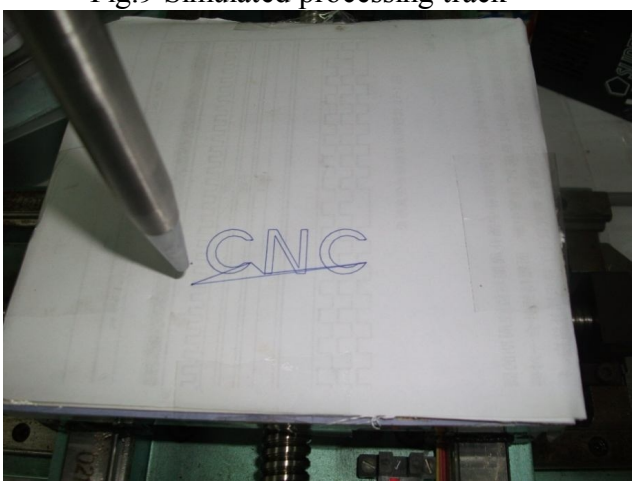

Fig.10 Actual running track

Conclusion

This paper discusses a development for hardware-configuration through redundancy of configuration circuit to implement the configuration with indefinite number of axes. The programmable card based this configuration construction has been used in open software CNC, which is autonomously developed by ourselves. An experiment preliminary validation viability and availability of Hardware-configuration circuit through load device driver program accomplish the debug of CNC milling. This design scheme has follow advantages：(1)Normal user has no need operate for loading Hardware configuration information and could initialize the hole system just by operate on the HMI. (2)Expert user will more flexible without be confined to any motion card profit from configuration construction of Hardware which is autonomously developed. Tentative the maximum configuration axis is eight based on programmable card internal resources and flexible flaw of Hardware resources distribute issue.

Acknowledgment

The author would like to acknowledge the support of the special subject of the national Nature Science Foundation of China. (No.51405085 and No.51175086).
This work is supported by youth scientific research personnel training funds of Fujian Jiangxia Univercity.(NO. JXZ2014006)

References

[1]. Koren Y.Reconfigurable manufacturing system having a production capacity method for designing same and method for changing its production capacity. United States Patent. 2003.

[2]. Bi Z, Lang S, Shen W. Reconfigurable manufacturing systems: the state of the art. International Journal of Production Research. 2007, 46(4):967-992.

[3]. Bi Z, Sherman Y, Lang T, et al. Development of reconfigurable machines. The International Journal of Advanced Manufacturing Technology. 2008, 39(11): 1227-1251.

[4]. Padayachee J, Masekamela I, Bright G, et al. Modular Reconfigurable Machines Incorporating Modular Open Architecture Control. In Proc of Mechatronics and Machine Vision in Practice. 2008:127.-132.

[5]. Moon Y. Reconfigurable Machine Tool Design. Reconfigurable Manufacturing Systems and Transformable Factories. 2006, pp:111-139.

[6]. Schreyer M, Tseng M. Design Framework of PLC-Based Control for Reconfigurable Manufacturing Systems. In Proc of International Conference on Flexible Automation and Intelligent Manufacturing (FAIM 2000). 2000, (1):33-42.

[7]. Luis.Morales, Velazquez, and Rene de Jesus : Open-architecture system based on a reconfigurable hardware–software multi-agent platform for CNC machines. Journal of Systems, Architecture, Vol.56(2010),p.407-418.

[8]. Wang Tao,Wang Liwen,Liu Qingjian : Research on software-hardware co-design of reconfigurable CNC system, Advanced Materials Research, p.458-463. (2011)

[9]. Wang Wen, Qin Xing, Chen Zi-chen : Research on reconfigurable CNC system based on programmable logic device, Computer Integrated Manufacturing Systems, Vol.8(2008),p.565-569.

[10]. Ren Zhi-ying, Chen Jian-xiong : Data sampling interpolation based on first off-line interpolation, Machine Tool & Hydraulics,Vol.37(2009),p.47-49.