The Research of Video Image Overlay Based on DM6446 Platform

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Abstract—With the rapid development of modern industry, the video detection technology is used more and more widely. In the video detection technology, the video image superposition technique occupies the most important position. This paper proposes a system based on video image overlay of TMS320DM6446, and makes information superpose to the target image. The whole system can be divided into camera module, video decoding module, DSP video processing subsystem module, LCD display module, and power supply module. In this paper, the system will be introduced from two aspects of hardware and software system, and the basic requirement of the system is implementation.

Keyword—Video Image; Superposition; TMS320DM6446; Video Decoding; Video Processing Subsystem

I. INTRODUCTION

With the rapid development of communication technology and computer technology, modern digital signal processing theory technology is becoming more perfectly, and the image processing technology is widely used in scientific research, industrial production, military technology and other fields. As people hold more and more highly attitude to the requirement of technology, simple image processing could not meet the demand, and begin to influence modern production in the guarantee of the quality system gradually. Therefore, video technique plays an increasingly heavy role in image processing, and especially the video detection technology which is developed by combining with video technology and computer technology, and it is a great extent improvement of the automation level and intelligent level of the production line. The video detection system replaces people to participate in more and more works by using image processing and computer technology. It greatly improves production efficiency and meets the needs of modernization. In the process of video detection technology application, people often put the different parameters and the image shown in the same video image, then analyze them. This would require the image superposition technique, which plays an important role in the video detection technology.

In the previous video overlay system, people usually adopt stack chips image processing. Although stack chips can solve the problem of character, it could not well done some image overlay, such as curve, the block diagram of the stack. Because of these problems, this system completes the image preprocessing by putting TMS320DM6446 chip as the core. The system isolates line sync signal and field synchronization signal through the video decoding chips TVP5150PBS. Then it introduces the character, image of the video image by superposition of video processing subsystem (VPSS). Finally, the system displays the image display module through the LCD screen. This design can not only quickly achieve real-time display, but also save the hardware cost of the system.

II. THE PRINCIPLE

The beginning of the realization of the image stack is image transmission. The image is made up of two parts of light and shade, and it can be decomposed into several basic units which is named "pixel". If people want to transmit an image successfully, it is necessary to put it all pixels converted into corresponding electrical signals respectively, and then send them one by one. In the modern TV technology, it takes the method of order (take) transmit pixel. At the sender, the pixel turns into electrical signals according to the position of each pixel. Then it is sent to the receiver. At the receiving end screen, each pixel appears one by one too. If people want to get the correct image on the screen of the receiving end, therefore, it should meet two conditions. Firstly, the time of the sender sends a signal which should be equal to the scanning time of the signal receiving end. Namely, the scanning frequency is consistent. Secondly, the starting scanning time of each line sync signal and each vertical sync signal should be consistent every time. At present, at the time of the video signal in transmission, the image signal, and blanking signal and the composite sync signal are mixed together according to certain proportion. Then the signals are sent to the receiver to control the movements of the electron beam scanning display tube and to ensure the position of each pixel in the image on the screen to display correctly. The TV system is the PAL television system in China, the horizontal scanning line 625, 25 frames per second, interlaced scanning every 0.02 seconds. Its horizontal synchronization signal and the vertical sync signal basic waveform are shown in Fig. 1[1].

In this system, the requirements of video image through camera superpose some other information on old images, such as square, round, segment, etc. Besides, the user can also add information by keyboard program modification.

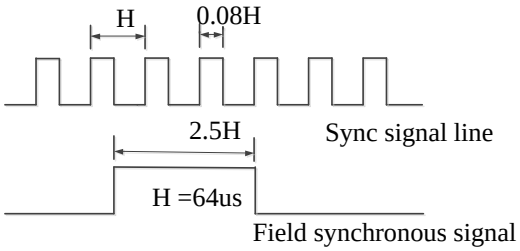

Figure 1. Sync signal waveform

According to these requirements, the system captures video signals from the camera, stacks system some external information what it needs the external information and transmits to the receiver in the process of transmitting images. And the essential of overlapping is on the pixel level image overlay choose electrical signals for each pixel. And the difficulty of image overlay is how to determine pixel. The selections of pixel point location are divided into two kinds of methods. They are the way of the grey value computation through the change and the video signal processing to separate horizontal synchronization signal and the vertical sync signal. Here, this system adopts the way that the output of the video signal of the camera is decomposed into blanking signal and the composite sync signal. Then TVP5150PBS separates horizontal synchronization pulse signal and the vertical sync pulse signal. Thus controlling line, the vertical counter counts accurately, the system gets the pixel location accurately.

III. THE HARDWARE DESIGN

This system bases on TMS320DM6446 (hereinafter referred to as DM6446) processor. DM6446 uses the DaVinci technology by TI Company. It is a video chip with high integration of multimedia processing platform. DM6446 processor can support multiple operating systems and has a strong ability of operation. The processor adopts dual-core architecture of ARM and DSP. Among them, ARM processor uses a nuclear of ARM926EJ–S whose work frequency is 297 MHZ. The DSP nuclear adopts TI high-end DSP series of TMS320C64X+ processor by Ti Company whose work frequency is 594 MHZ. In addition, DM6446 includes rich on-chip peripherals and other peripheral parts.

DM6446 microprocessor structure diagrams are shown in Fig. 2 below.

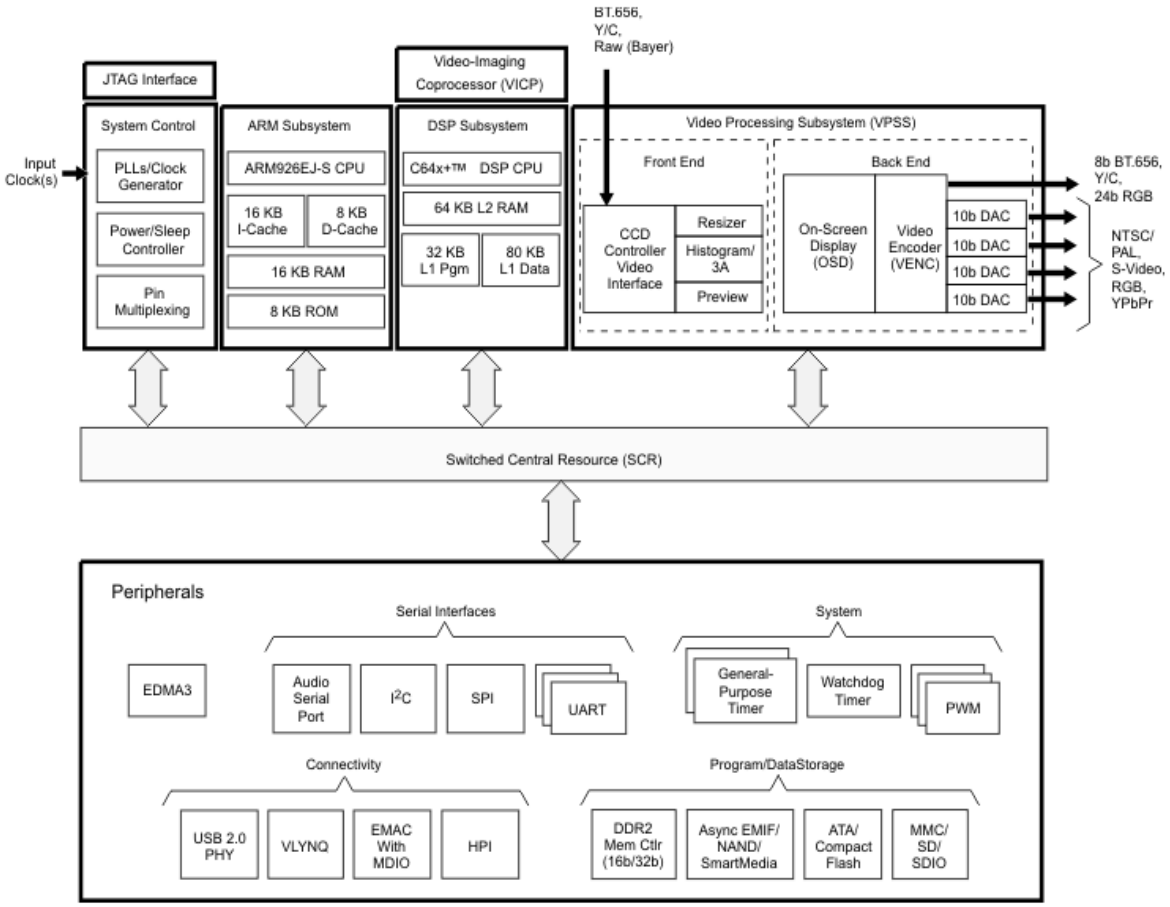

Figure 2. DM6446 microprocessor structure

This system is composed of camera module, video decoding module, DSP video processing subsystem module, LCD display module and power supply module. Camera module collects the external video signal and

transmitters to the video decoding module. The video decoding module separates the video image signal into horizontal synchronization signal and the vertical sync signal through the video decoding chip TVP5150PBS. The video processing subsystem module superimposes some information to the horizontal synchronization signal and the vertical sync signal pulse, such as images, symbols. Finally the output of superposition images display on the LCD liquid crystal display module. The system composition block diagram is shown in Fig. 3.

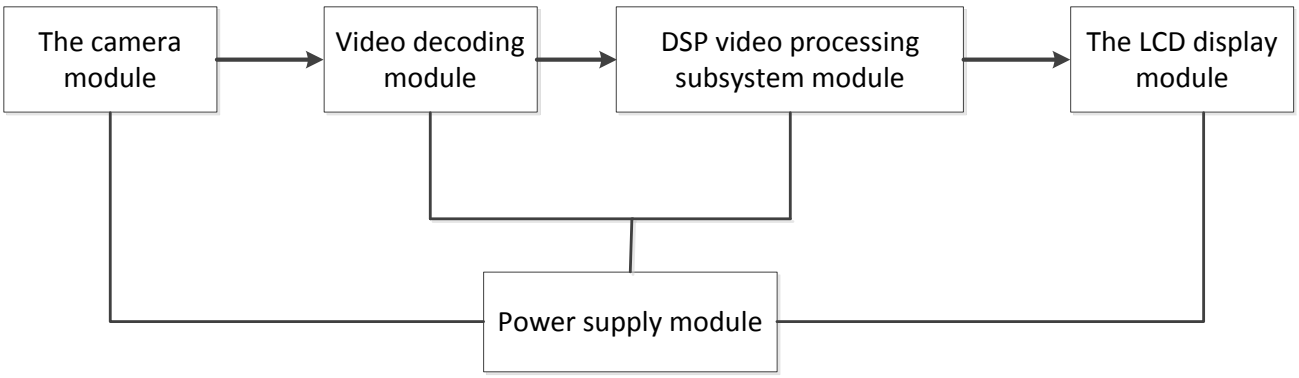

Figure 3. System composition block diagram

A. *Camera module*

The camera module uses CCD image sensor. It can directly convert photochemical signals into analog current signal. And current signals via amplification and modulus conversion,realize image acquisition, storage, transmission, processing, and returned to the show. This system adopts the TD - 2073 CCD camera. As shown in Tab 1.

TABLE I. CCD CAMERA

Camera CCD	Sony Color CCD
Power	DV12V
Sensor	1/3 inch Sony Color CCD
Video Format	PAL/NTSC
Resolution	600TVL
S/N Ratio	≥50dB

B. *Video decoding module*

In addition to containing the image information, it also contains the line sync signal, blanking signal, vertical sync signal and field blanking signal, etc through the video camera. If you want to acquire the video signal, you must process the video signal, separate into horizontal synchronization signal and the vertical sync signal and line, blanking signal. The video decoding chip of this system is TI TVP5150PBS chip produced by Ti Company. As shown in Fig. 4.

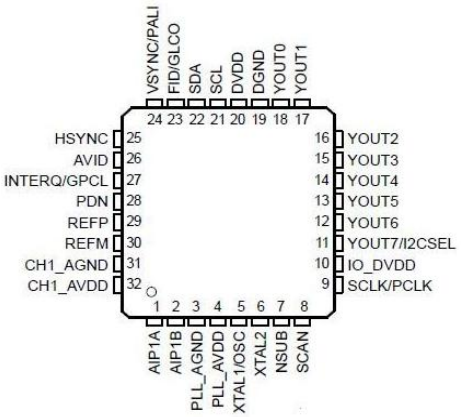

Figure 4. TVP1550 pin figure

TVP5150PBS adopts all 32 feet encapsulation, and it is a video decoder of high performance and low power consumption. TVP5150PBS chips use 14.31818MHz as the input clock. Analog and digital input voltage is 1.8 V and I/O port voltage is 3.3 V. It supports a variety of formats signal, and can convert Video signals into YUV4:2:2. It supports two composite Video (CVBS) or an S-Video input (Y/C). The output format is the ITU-R BT. 656, and this format does not need to output line sync signals, and filed synchronization signal. A start and end of the format are indicated through the identification code which is embedded into the image data. TVP5150 chip signal input has two roads of APIP1A and APIP1B. And they have the impedance matching design to prevent the reflection of the input signal. AVID is TVP5150 proprietary signals, and is the "light" of the effectively video data. Through register Settings, controling the start and end time of AVID means controling the output of the part of images which will be intercepted.YOUT [0:7] has 8 byte YCbCr signals outputs. The field synchronization signal choose pin HSYNC and VSYNC as output. PCLK/SCLK pin transmits 13.5MHz and 27 MHz clock signal to DM6446 chip which are used to collect

synchronize data. TVP5150PBS completes configuration through standard I2C bus. For TVP5150PBS decoder, I2C bus is an indispensable part. I2C bus of TVP5150 is composed of dta line SDA and clock line SCL, and it can send and receive datas. In the process of data transmission, the I2C bus has three types of signals:

- The start line (Start) When SCL is high level, SDA becomes from high level to low level, and begins to transmit datas.
- The end line(Stop) When SCL is low level, SDA becomes from low level to high level, and stops to transmit datas.
- The answering signal (AcK) When the I2C of received data which receives 8 bits of datas sends specific low level pulse to the I2C of sending datas, and it means receiving datas.

It is important to note that when the I2C bus transmits datas, it must guarantee the stability of data on the SDA and SCL is high levels, or the data would be sentenced to start or end signal. Its data transmissions of the data formats are shown in Fig. 5 below.

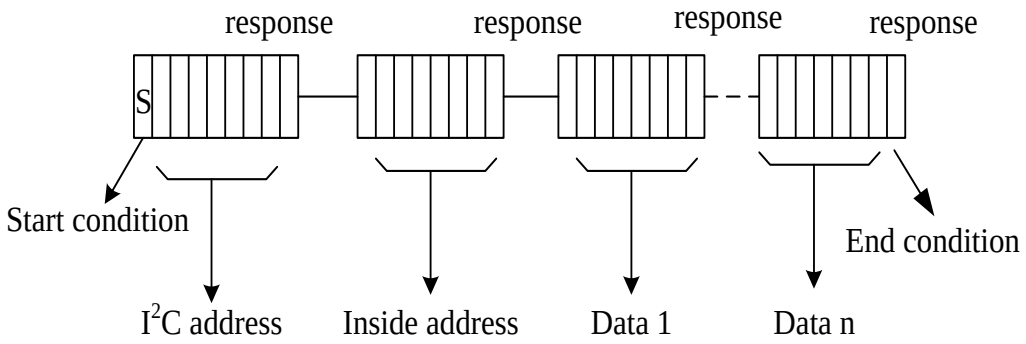

Figure 5. I2C data transmission formats

Here, the I2C bus data transfer rate can reach 400 Kbit/s. In this article, because of the system adopting a SEED-DVS6446 experiment box, DM6446 system contains two pieces of TVP5150PBS chip. Now the experiment box takes data transmission of TVP5150PBS configuration.

a) By the I2C bus master device, DM6446 sends starting conditions.

b) DM6446 sends the device address (TVP5150 address 0xBA or 0xb8), indicates the write operations, and waits for the TVP5150 response.

c) After receiving the TVP5150 response, DM6446 sends conFig. register address, waits for the response from the device.

d) After receiving the TVP5150 response, DM6446 transmits system to register configuration written or read data, waits for a response.

e) After receiving the TVP5150 response, DM6446 sends stopping bit marks of the end of this time configuration.

C. DM6446 video processing subsystem module

DM6446 processor provides a video processing subsystem (VPSS). VPSS works are the responsible hardware module for video input and output of DM6446. And it has the advantages of a fast calculation speeding, the using of high performance and the small CPU. VPSS works include video processing front end (VPFE) and video processing back end (VPBE) which are respectively used for external image input device and video output device. The structure diagram 6 as follows.

VPFE module is mainly used to capture video signal or directly from the front end of the existing video signal. It is composed of CCD controller, image preview, H3A controller, the size of the window regulator, the histogram of the generator. The top three produce preview images with the required resolution based on the input video, the latter two support automatic focus, the closed-loop automatic white balance, automatic exposure. And CCD console can connect with a CCD camera, CMOS sensor or a video decoder. It supports the bell template data and the YUV4:2:2 data format after decoded. VPBE is composed of OSD (On Screen Display) module and video encoder (VENC), which are the two main modules. VENC contains digital LCD (DLCD) and analog (DAC) interface. The DAC interface works in 54 MHz, and supports a variety of standard format of the output, such as PAL system and NTSC system. VPBE supports two video windows, two OSD windows, and a pointer (cursor) window. As shown in Fig. 7.

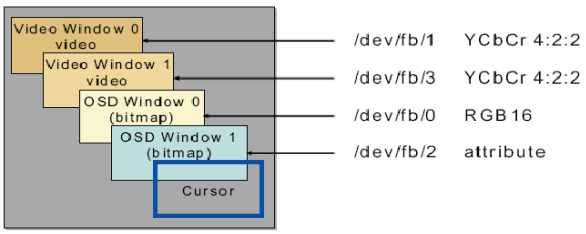

Figure 6. OSD module windows

OSD engine can work with two independent video windows, two independent OSD windows. The second OSD window can also be configured to properties window to control video window and mix the first OSD window. And the properties window can also support 8 permeability of mixture. The OSD module displays data (image,

character and other data) which is superimposed on the video image data, and then is transmitted in YCbCr format (VENC) to the video encoder to encoded output. When the video is outputed, DM6446 processor adopts DM6446 on chip four road 110 - bit DAC outputs, and it can realize the CVBS and VGA outputs. Among them, the CVBS output interface occupies 1 road DAC, and the VGA output interface takes 3 road DACs.

Through TVPS5150 decoders decoding into YUV4:2-2 format of video data, the system analog video signals are sent to VPFE CCD controller. And then the data which exists in the VPSS works internal Buffer temporarily are transmitted to the external DDR SDRAM memory through the EMIF interface . VPBE screen display (OSD) module delivers the video data in the form of YCbCr to video encoder (VENC), and transmits the output to the VGA or CVBS through video encoder interface.

D. Power supply module

With the rapid development of semiconductor technology, semiconductor companies mostly put low voltage integrated circuit as the object of promoting, such as high-end DSP, FPGA and ARM products which have been widely adopted 3.3 V ~ 1.5 V power supply. This system uses a SEED - DTK6446 experiment box, and the design of the power module adopts 5 V / 3.3 V power supply.

IV. THE SOFTWARE DESIGN

According to the system requirements, system software module is divided into camera module, video decoding module, DSP video processing subsystem module, LCD display module.The software design of this system adopts the method of assembly and C language programming. For high speeding requirements, time being little, and parts of the driver code, people use assembly language. And for the main program written use C language which are to meet the requirements of the program readability, modular.

After the system is powered on, DSP begin to initialize. Power is on reset, ARM starts from initial space executable program, DM6446 system begin as the program to complete the initialization. It includes changing processor running mode, the CPU initialization, each module in the system initialization (DDR2 memory controller initialization, selection signal of PLL1 and PLL2 initialization, system initialization, etc).

In addition, people should also deal with peripheral equipment program design. In peripheral equipment applications, video module design is the most important part of the module designs. Video module design includes video decoding chip TVP5150 initialization, video processing front end initialization, video processing back-end initialization, image display, etc. Fig. 8 is the video module design flow chart.

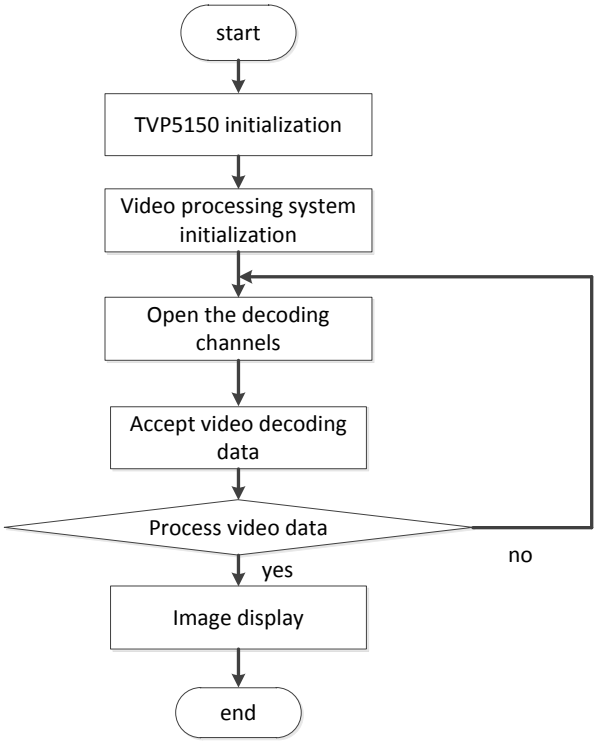

Figure 7. Video module design flow chart

A. Image acquisition module

The system completes the video acquisition through the front end of the CCD camera, and the collected frame image data transmits to the TVP5150 and proceeds A/D conversion. After TVP5150 converts a frame image data, data will be taked by acquisition thread. And let compressed thread and display thread will compress and display datas which is in Buffer.

The main function call pthread_create function to create video acquisition thread and set the thread main function entry address. After it succeed, the system will jump to the entry address automatically.and start to perform video collection procedures.

Video acquisition operation process is as follows:

Open the video acquisition device.

```
#define V4L2_DEVICE     "/dev/video0"
…
Fd=open(V4L2_DEVICE,O_RDWR|O_NONBLOCK, 0);
```

Initializes the acquisition equipment.

```
captureFd=initCaptureDevice(&capBufs,&numCapBufs, envp->svideoInput,envp->imageWidth, envp->imageHeight,0);
```

TVP5150 chip initialization is mainly done through the I2C bus. Firstly, it should select the video input channels. When the input signal is a Composite signal, it can choose channel A or B. But if the input signal is S-Video signal, the input of channel A is for the Luminance signal and the channel B is Chrominance signal.Besides, the signal's output format is 8-bit ITU-R BT. 656.

B. Video processing subsystem module

Video processing subsystem includes video processing front end (VPFE) and video processing back-end (VPBE).

VPFE interface is made of CCD controller, the preprocessor, columnar module, automatic exposure /white balance/servo module (H3A) and register. VPBE is composed of video encoder (VENC) and OSD module. The main function of OSD module is mixed video data and display data and sends the signal to the VENC module to code and in YcbCr format output image. Finally, the output images are displayed in the LCD display.

For the operation of the OSD module, the system adopts Fbdev device driver to realize the superposition of output of the video image.

Firstly, define the display device.

```
#define OSD_DEVICE      "/DEV/FB/0"
#define ATTR_DEVICE     "/DEV/FB/2"
#defineFBVID_DEVICE     "/DEV/FB/3"
```

Secondly,operate various windows

```
Fd = open(OSD_DEVICE,O_RDWR);
…
Fd = open(ATTR_DEVICE,O_RDWR);
…
```

V. THE RESULTS

In order to detect stack performance of the system, the system adds symbols and other information in the collection of the video image. As shown in Fig. 9 below.

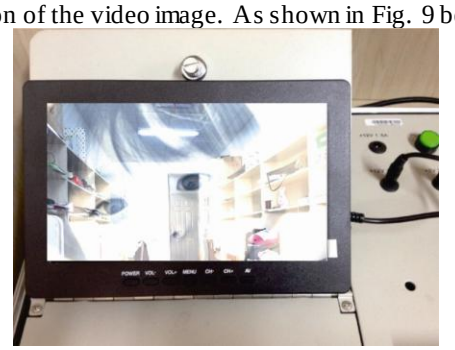

Figure 8. Video image superposition results

As you can see, other image information is superimposed on the video image. This system is well completed the video image overlay, and it can be at ease using. In practice, of course, the system can also superpose different characters and image information at other locations in the video image according to the different requirements.

VI. CONCLUSIONS

Video detection technology with the vigorous development of the modern industrial production is used more and more widely, and video image superposition technology plays a more and more important role in video detection technology. Taking TMS320DM6446 application platform as the core, this paper puts forward the video image stack system. The article has respectively carried on the detailed introduction from two different directions hardware and software on the system. With DM6446 models of DSP to realize the system function, the system improves the real-time performance of the system, reduces the cost, and makes the system reliability be greatly enhanced.

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