A Low Dropout Regulator with Low Quiescent Current

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Abstract—This paper introduces a low dropout regulator (LDO) by bipolar process. This LDO is composed of a starting circuit, a bandgap reference, an amplifier and power transistors. The bandgap produced a reference voltage about -1.25V, this voltage will be amplified to -5V by the error amplifier, power transistors and feedback resistances, and the output of the amplifier provides the drive current to the power transistors to carry 1A load current. The starting circuit provides current to the constant current source to ensure the work of the internal structures. The bandgap, enable circuit, error amplifier and the output circuit are analyzed respectively. Through simulation results, it can be seen the output current of this regulator is 1.0A, and the typical quiescent current of this regulator is below 2mA, the method to reduce the quiescent current is presented.

Keywords- Quiescent Current; Bandgap; Power Transistors; Low Dropout; Output Current

I. INTRODUCTION

Low dropout linear regulator, also known as the LDO linear regulator, is a kind of DC linear regulator which the input voltage and output voltage difference is very low. As an important member in the field of power management, it has higher power conversion efficiency than the traditional linear regulator, and it has more simple structure, lower cost and lower noise than the switching regulator. The low dropout linear regulator has advantages of fast input and output response, few external components and convenient use, etc., so it is widely used in mobile phone, PDA, digital cameras, notebook computers, MP3/4 and other portable electronic products and it has broad market prospects[1-3].

An LDO is characterized by its drop-out voltage, quiescent current, load regulation, line regulation, maximum current (which is decided by the size of the pass transistor), speed (how fast it can respond as the load varies), voltage variations in the output because of sudden transients in the load current, output capacitor and its equivalent series resistance. Speed is indicated by the rise time of the current at the output as it varies from 0 mA load current (no load) to the maximum load current. This is basically decided by the bandwidth of the error amplifier. It is also expected from an LDO to provide a quiet and stable output in all circumstances (example of possible perturbation could be: sudden change of the input voltage or output current). Stability analysis put in place some performance metrics to get such a behaviour and involve placing poles and zeros appropriately. Most of the time, there is a dominant pole that arise at low frequencies while other poles and zeros are pushed at high frequencies[4-7].

As shown in Fig. 1, low dropout linear regulator (LDO) structure mainly comprises a starting circuit, constant current source bias unit, enable circuit, adjusting element, reference, error amplifier, feedback resistor network and protection circuit, the basic principle is this: when the system is powered up, if the EN is at a high level, the whole circuit starts on, the constant current source circuit provides bias current for the whole circuit, a reference voltage established, the output rises with the input, when the output reaches the set value, the output feedback voltage is close to the value of the reference voltage, at this time, the error amplifier will amplify the error signal between the feedback voltage and the reference voltage, this amplified signal will be adjusted by the output transistor, thus this process forms a negative feedback, to ensure the stability of the output voltage to a predetermined value, if the input voltage or output current changes, the closed loop will keep the output voltage constant[8-11].

$$V_{OUT}=（R_1+R_2）/R_2 \times V_{ref} \quad （1）$$

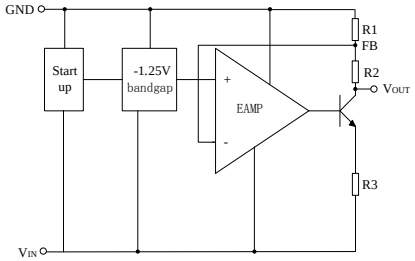

Figure 1. the basic circuit of low-dropout regulator LDO

Quiescent current is an important part in designing a low power waste, low operating supply current electronic devices. Assume the input current of LDO is I_{IN}, the output current is I_{OUT}, and the quiescent current of LDO is:

$$I_Q=I_{IN}-I_{OUT} \quad （2）$$

Quiescent current reflects the power waste of the internal circuits in LDO, in order to get the best current

efficiency and reduce the current waste of the internal circuits, and the quiescent current must be as lower as possible. Quiescent current consists of bias current of regulator (the consumed current of reference voltage, the sampling resistor and the error amplifier) and the drive current of the base of the regulator. The quiescent current depends on the regulator, the configuration of LDO and the environment temperature.

Generally, the quiescent current in bipolar transistor will increase in proportion to the load current, because bipolar transistor is driven by current. However, bipolar transistors have abilities of good amplification and high switching speed which can't be replaced by MOSFET.

In this circuit, there is a diode connected between the output circuit and the power transistor driven, when the dropout voltage between input and output get a little increase in this LDO, the diode will be turned on, then the drive current of power transistors is not from the internal circuit any more, it is all from the load current, so this structure can reduce the quiescent current dramatically, and also reduce the power consumption of the whole LDO.

II. CIRCUIT DESIGN

This LDO is composed of a starting circuit, a bandgap reference, an amplifier and power transistors. Its working principle is as follows: the bandgap produced a reference voltage about -1.25V, this voltage will be amplified to -5V by the error amplifier, power transistors and feedback resistances, the output of the amplifier provide drive current to the power transistors to carry 1A load current. The starting circuit provides current to the constant current source to ensure the work of the internal structures.

A. Bandgap

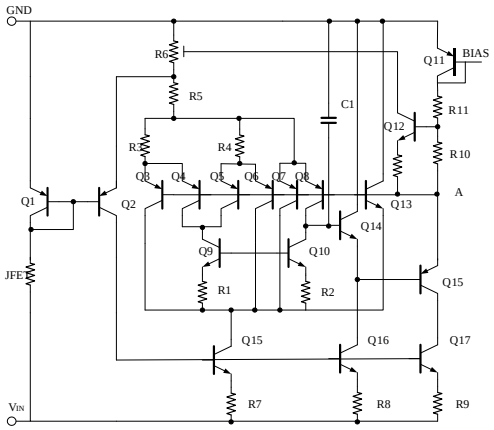

Figure 2. Circuit of Bandgap

Fig. 2 shows the circuit of bandgap. When the circuit is powered on, the JFET is equivalent to a constant current source, then Q1 and Q2 turns on, Q15 turns on since Q2 provide a base current for it, then the bandgap starts to work, when the bandgap voltage establishes, the emitter voltage of Q2 increases, Q2 turns off. The function of Q14 and Q15 is to stabilize the bandgap voltage. If the voltage of point A increases, the base voltage of Q14 decreases, the emitter voltage of Q14 (the base of Q15)also decreases, and the emitter voltage of Q15(point A) decreases, according to this negative effect, the voltage of point A is steady.

B. Enable Circuit

Fig. 3 shows the circuit of enable circuit ,when the potential of EN is below 0.8V, the emitter potential of Q2 and Q4 is negative, the base potential of Q2 and Q4 is also negative, so Q1 and Q3 turns on, Q7 turns off, then the LDO will work. When the potential of EN is above 2V, the base potential of Q2 and Q4 is positive, so Q1 and Q3 are turned off, Q2 and Q4 are turned on, then the base potential of Q10 turns on Q10, the connector of Q10 control the work of LDO, and the LDO is closed.

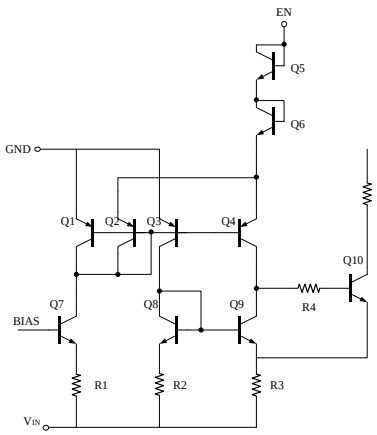

Figure 3. circuit of enable

C. Error amplifier

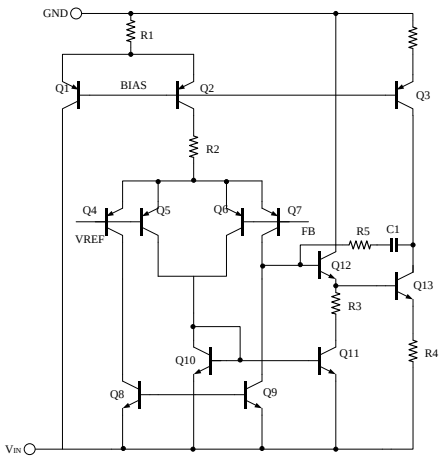

Figure 4. circuit of error amplifier

Fig. 4 shows the circuit of error amplifier, Q2 provides bias current for the error amplifier, Q4, Q5, Q6 and Q7 work as the input of the error amplifier, the reference voltage input to the forward port, the feedback voltage input to the reverse port, Q8 and Q9 are the active load of the error amplifier. The output signal of the EA is buffered by Q12, and then amplified by Q13 to output a driving signal of the power transistors. A Capacitance connected between the two stages of EA is used for the compensation effect.

D. The Output

Fig. 5 shows the circuit of output, When the circuit works in low dropout voltage region, the output signal of EA passes through Q5, arrives at the base of Q15, at the same time, this signal is also through the base of Q6, since Q6 is turned on ,the Q3 and Q4 are turned on, also Q14 is turned on, Q14 provides connector current for Q15, Q15 drives the power transistors. Q12 and Q13 are the keys to reduce the quiescent current, if the dropout voltage of input and output get increase, Q13 is turned on, then the emitter potential of Q14 raises, Q14 is turned off, at this time, the drive current of power transistor is provided by load current, so this structure can reduce the quiescent current sufficiently, and the power consumption is saved.

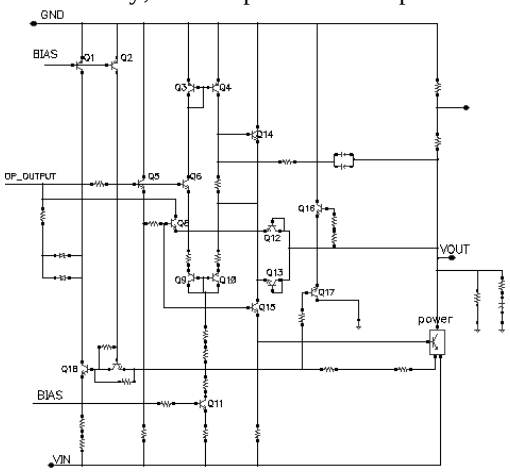

Figure 5. circuit of output

III. SIMULATION

Under the condition of 6μm feature size and 35V maximum working voltage, the quiescent current of the circuit is simulated by cadence, the simulation condition is typical process condition, V_{IN}=-10V, C_O=47μF, $I_O \leqslant$1A.

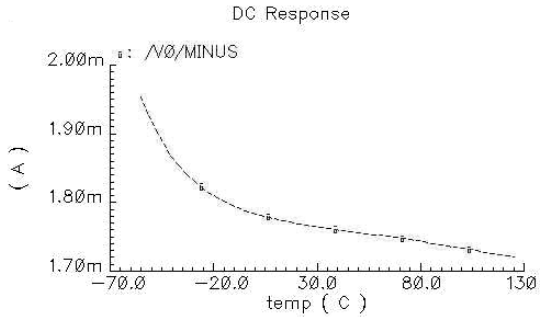

Figure 6. the quiescent current with Q12 and Q13 in the output circuit

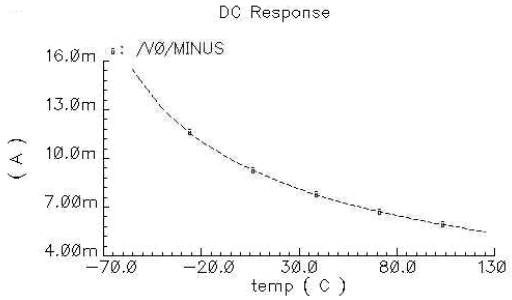

Figure 7. the quiescent current without Q12 and Q13 in the output circuit

From above two charts Fig. 6 and Fig. 7, the quiescent current is much greater when there is no Q12 and Q13 in the circuit.

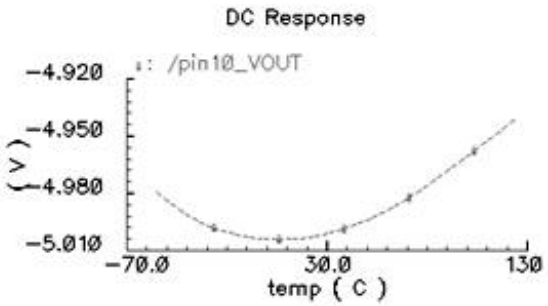

Figure 8. the output voltage of the LDO at difference temperature

From the above picture Fig. 8, when the output current is 1A, the output voltage is stable at 5V in the specified temperature range.

IV. THE LAYOUT

This LDO is a power device, the output transistors are arranged symmetrically to avoid overheating of the chip. As shown in Fig. 9. The size of the chip is 3.90mm*2.70mm.

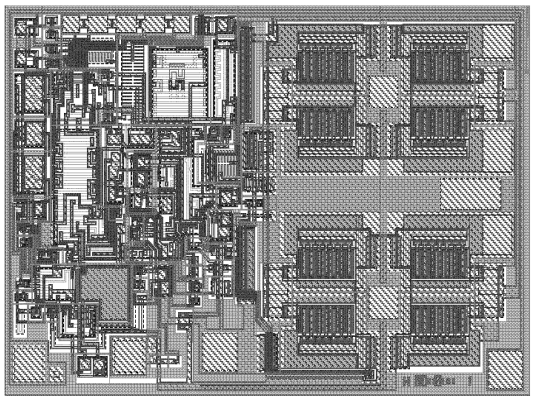

Figure 9. the layout of this LDO

V. RESULT

This LDO has 6 pins so it is packed in D08S, it works between －40℃ to ＋85℃, the main electrical characteristics are as below:

Work voltage：-10～-26V；reference voltage：-1.25V±1%； output current：1A；output voltage：-5.10V～-4.90V；Quiescent current≤3mA。

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