A Novel Traffic Generator for Switch Testing

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***Abstract*—Traffic generator is a key component in the verification and test platform for network switches. It can produce packets for different network protocols, and the generated traffic can simulate the real internet traffic. A novel traffic generator, different from general traffic generator structure, is implemented by software and hardware co-design methodology, which using software to generate the complex traffic types and hardware to generate corresponding packets. The proposed traffic generation solution is able to meet the requirements of the today's high-speed, high-load, complex network. The traffic generator is developed based on Xilinx Virtex-5 FPGA development board with Uniform, Poisson and MMPP traffic models at Gbps line rates, and verified on test platform.**

Keywords-traffic generator; traffic model; switch, FPGA

I. INTRODUCTION

Nowadays, switches play a very important role in the exchange of information and data transmission. As the basis of modern network system, their performance usually can determine the performance and stability of the network system. Therefore, how to test switches has become an important topic of researches on the switch.

Traffic generator can produce packets for various network protocols, and the generation of traffic aims for simulating the real network traffic. The fundamental requirement for a traffic generator is that it can efficiently verify functionality and locate the error for switches in the design phase, also can test the performance at the application stage.

Currently, the traffic can be generated by PC software[1] or special test equipments[2,3]. Software-based traffic is flexible, inexpensive and can be subject to a variety of models. However, with the increase of the number of switch ports, their transmission rate decreases linearly because of the bandwidth limit between hardware and software. Special test equipments can solve the problem of transmission rate, but are generally very expensive and is not suitable for academic research purpose. Our solution is based on SoC structure and software and hardware co-design methodology, which absorb the advantages of above two mentioned solutions[4,5].

The proposed traffic generator is also developed with SoC structure based on Xilinx Virtex-5 FPGA development board, which generates the traffic of uniform, Poisson and MMPP types at Gbps line rates.

II. THE STRUCTURE OF PROPOSED TRAFFIC GENERATOR

Figure 1 shows the basic structure of the proposed traffic generator. We divided the hardware and software for uniform, Poisson and MMPP traffic model, and chose Power PC 440 as microprocessor, which is implemented as a hardcore in Xilinx Virtex-5 FPGA.

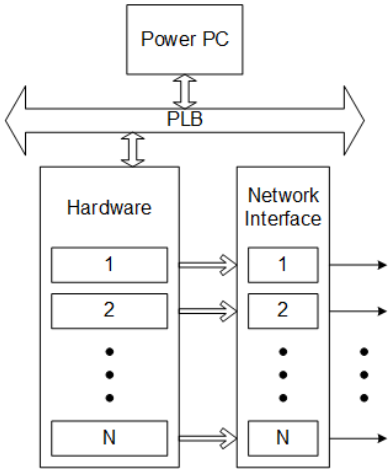

FIGURE I. THE TRAFFIC GENERATOR'S STRUCTURE

The software of traffic generator running on Power PC generates configuration and parameters of each packet based on traffic models. The configuration defines the format of all packets, the distribution of packets' destination address. And the parameter defines length and departure time of each packet. Then, the hardware of traffic generator generates corresponding packet at a specified time. The network interface module, which is also implemented in FPGA, translates the packet form hardware of traffic generator into particular protocol.

III. The Hardware Implementation

The hardware of the traffic generator is adopted to generate an entire packet and send it to network interface module at a specified time. The hardware architecture is designed as a custom IP by Verilog HDL. We can copy the IP to apply to multi-port test. Figure 2 illustrates the hardware architecture of our one-port traffic generator. It mainly includes interaction module, protocol module, etc.

The interaction module is the interface between the custom IP and Power PC applying the PLB bus protocol. It receives configuration and parameters of traffic models from the software.

The protocol module fills the packet contents for supporting a particular network protocol.

The D_ID module generates destination addresses of the packets submitting to a certain distribution model, such as uniform distribution.

The length module controls the packet length. As the same as the D_ID module, the distribution of the packet length can be determined by the LFSR module.

According to the protocol type, D_ID, packet length and other information, the filler module will encapsulate a packet and store it into a queue.

The interval FIFO stores the departure time of the packet calculated by software. The departure time of current packet is defined as the number of interval period after the time of previous packet.

The correction module modifies and updates the actual departure time of each packet. If a departure time is less than the corresponding packet length, the departure time will be replaced by the packet length.

The transmission module sends packets from the filler module to the network interface module at the time given by the correction module.

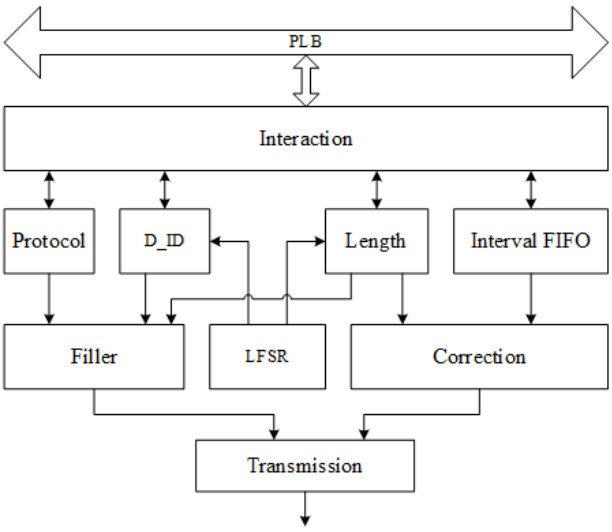

FIGURE II. THE HARDWARE ARCHITECTURE

IV. The Software Implementation

The traffic generator supports three traffic models — uniform, Poisson and MMPP. The software of the traffic generator provides a user interface to select traffic model, load and corresponding parameters, like the probability of off state to the on state in MMPP.

The second function of the software is generates configuration and parameters of each packet based on these traffic models, load and corresponding parameters. Then, parameters will be sent to the interactive module through the PLB bus. The workflow of the software is as follows:

step.1 Set traffic model, load and corresponding parameters.

step.2 Initialize each IP of the SoC through the PLB bus, such as DDR, cache, etc;

step.3 Initialize configuration of the hardware for generating packets, include protocol, the distributions of D_ID and packet length;

step.4 Generate the parameters of the packet and transfer them to the interactive module

step.5 Analyze the status of the interaction module. If the parameters is not loaded by the interaction module, the software waits. If loaded, proceeds to step.4.

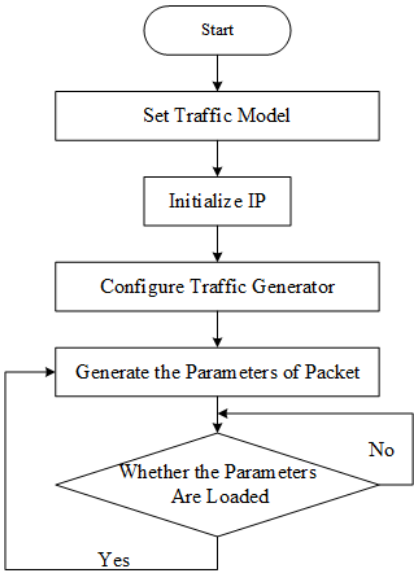

FIGURE III. THE SOFTWARE PROCESS

V. The Traffic Models and Validation of the Proposed System

In order to accurately assess the performance of a switch, selecting a suitable traffic model becomes particularly important. After analyzing the characteristics of modern network, three traffic models — uniform, Poisson and MMPP, are selected from a number of distributions for the traffic generator.

1. The uniform traffic model generates packets at a constant rate according to a fixed load. For this model, the main task is to verify the transferring function between switch ports.

2. The Poisson traffic model is defined as the number of packet arrival n(t) in time series t subjecting to Poisson distribution with the parameter λt[6], as shown in

$$P_n(t) = \frac{e^{-\lambda t}(\lambda t)^n}{n!} (n = 0,1,2,\cdots,n) \quad (1)$$

The corresponding packet arrival time T subjects to negative exponential distribution, as that is $F(t) = 1 - e^{-\lambda t}$. The Poisson model is similar to the traffic behavior of low-load, low-burst and small-scale networks.

3. Markov Modulated Poisson Processes (MMPP) is a common one of Markov models. It is a double random process superimposed on the Poisson process with a parameter λ and the update process with a parameter υ[7]. The MMPP model has autocorrelation and high bursty features. It can describe the traffic behavior of high load, high burst, and multi-service network types.

A switch supported Fiber Channel (FC) protocol has been tested under a test platform equipped with the proposed traffic generator. To verify whether the generated packets are consistent with the traffic models, we have designed a monitor to capture the packets and analyze them.

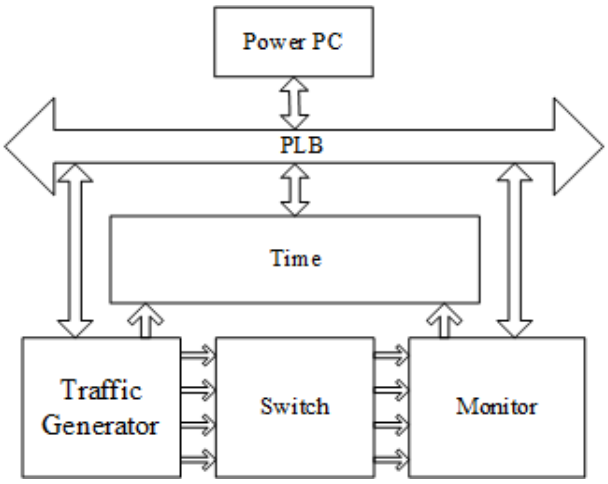

FIGURE IV. THE TEST PLATFORM FOR PROPOSED SOLUTION

Figure 5 shows the test results. In this experiment, the traffic load is set to 0.8, the packet length is 1000 bytes and test time is 10ms. The x-axis represents the n-th slot, and the y-axis represents the number of packets captured in the n-th slot. The results in Figure 5 are respectively for uniform, Poisson and MMPP traffic models from top to bottom. We can find that for the uniform model, the traffic generate can generate packets at a constant rate. Poisson traffic has burst behavior at a short scale, but tends to smooth at a long scale. MMPP traffic has a high bursty nature both in the short and long scale.

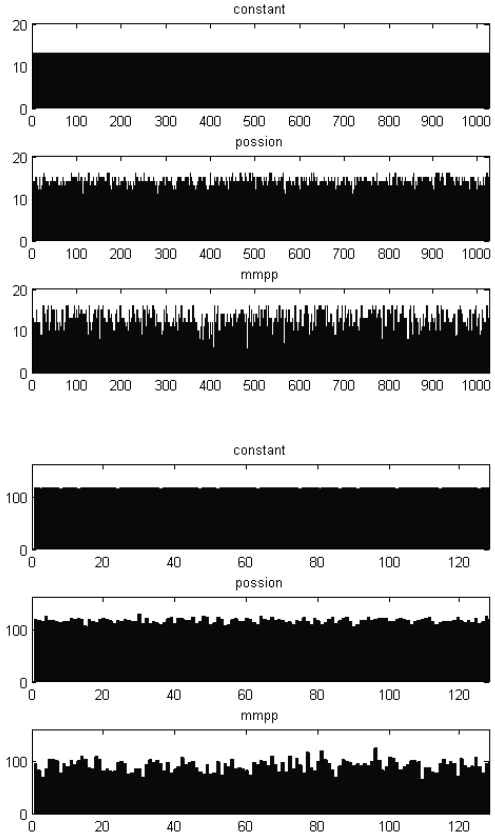

FIGURE V. TEST RESULTS OF TRAFFIC GENERATOR (LEFT) SLOT IS 0.1MS; RIGHT SLOT IS 0.8MS

VI. CONCLUSION

In order to test the switch supported FC protocol, we designed and implemented a traffic generator with uniform, Poisson, and MMPP traffic models. Then, we validate that the generated packets obey traffic models by our test platform. The traffic generator, based on SoC structure and software and hardware co-design, meets the needs of switch test under high-speed and complex network environment. It is also low-cost and easy to implement which can provide an effective solution to test switches.

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