Analysis and Calculation of Miller Capacitor in Amplifier for 8 Bits Pipeline ADC

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Abstract. This design pays much attention on analyzing and calculating Miller capacitor in operational amplifier to optimist OP (Operational Amplifier). The design for a 8-bit high speed, low power pipeline ADC is based on standard 0.18um CMOS technology, with 3.3 power supply. The results show that the dc gain of the operational amplifier is 96dB, the gain-bandwidth is 167MHZ, and the ADC can achieve 8bits resolution and 10M samples/s.

1.Introduction

System-on-chip (SOC) requires the integration of analog circuits and digital circuits on a signal chip. Recently, the applications for ADCs have expanded widely as many electronic systems that used to be entirely analog have been implemented using digital electronics [1]. It is very critical to design a high performance A/D converter, which is based on standard CMOS technology. Recently, the applications for ADCs have expanded widely as many electronic systems [2,3]. The pipeline ADC can achieve both high accuracy (6-14 bit), and high conversion speed (5MHZ-200MHZ) [4]. The pipelined ADC is serial work, but it is working in parallel from every step of the conversion [5]. So its total conversion rate depends on the maximum speed of a single-stage circuit, and the total conversion rate is no relation with the numbers of the stages. In this paper, we pay attention on analyzing and calculating Miller capacitor in operational amplifier to optimist the amplifier. So we design an 8-bit high speed, low power pipeline ADC based on the standard 0.18um CMOS technology.

2. Principle of pipelined ADC

In the high-speed and high precision ADC, the OP needs a high enough gain and gain bandwidth. In order to achieve the requirements, we used the fully differential CMOS operation amplifier and the gain improves technology. The OP is a two-stage CMOS operational amplifier, and it is showed in Fig.1. In Fig.1, it includes a differential input stage, a load capacitance C_L, and a stable transconductance bias circuit. Because the load capacitance C_L is often several pf, the output drive level is no need. The CMOS two-stage operational amplifier has many advantages: high voltage gain, rail-to-rail output dynamic range, a large common-mode input range, a Miller compensation capacitor, etc.. But its main drawback is the second pole (non-dominant pole) is determined by the product the load capacitance and the second amplifier output impedance, which reduces the bandwidth of the op amp. Another drawback is the OP has the right-half plane zero which is caused by the compensation capacitors from the feed-forward pathway. But the polar can be eliminated by selecting the appropriate compensated resistor: linear region of a NMOS (M14). We can achieve the zero point moving by adjusting its width to length ration and gate-source voltage. Because the op is the differential input, so the dominant pole compensation is mainly influenced by the Miller compensation capacitor Cc.

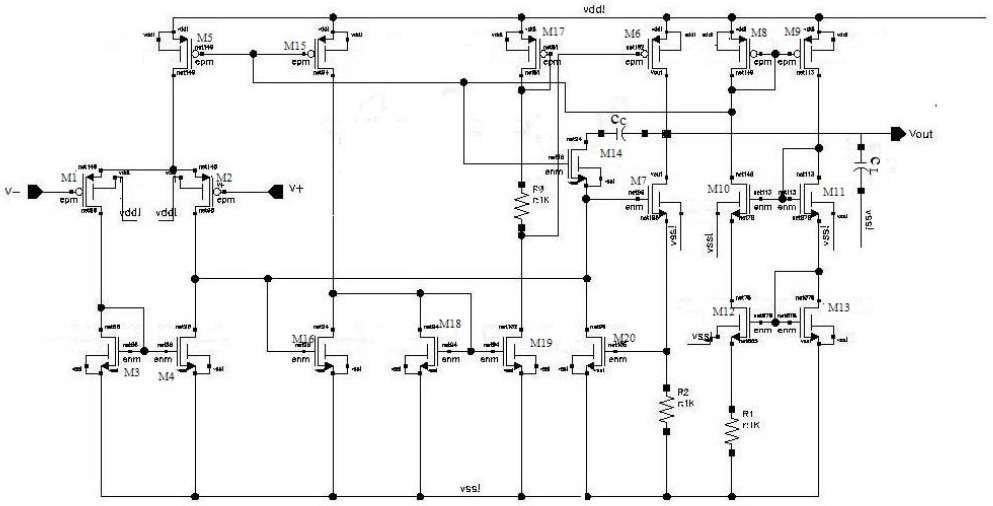

Fig.1 the structure of OP

The small signal model can simplify the calculation of the linear model, and it can be regarded as the ratio amount of the small changes in the large signal model parameters. g_m is the channel admittance, and in the saturation region it is:

$$g_m = \sqrt{(2K'W/L)|I_D|(1+\lambda v_{DS})} \approx \sqrt{(2K'W/L)|I_D|} \tag{1}$$

g_0 is the channel conductance for small signal

$$g_0 = \frac{I_D\lambda}{1+\lambda V_{DS}} \approx I_D\lambda \tag{2}$$

W is the effective channel width, and L is the effective channel length, λ is the modulation factor of the channel length（V^{-1}）.The first pole is :

$$w_{p1} \approx \frac{g_{02}+g_{04}}{(\frac{g_{m6}}{g_{06}+g_{07}})C_c} \tag{3}$$

Open loop gain is:

$$A_0 = \frac{g_{m1}}{g_{02}+g_{04}} \cdot \frac{g_{m6}}{g_{06}+g_{07}} \tag{4}$$

Unity gain bandwidth:

$$w_u = A_0 \cdot w_{p1} = \frac{g_{m1}}{C_c} \tag{5}$$

Because there is no DC current pass the NMOS tube M14, it works in the linear region, and it is equivalent of a resistor.

$$R_c = \frac{1}{\mu_n C_{ox}(\frac{w}{L})_{14} V_{eff14}} \tag{6}$$

The role of the M14 tube is to eliminate the right half zero which is introducted by the Miller capacitor Cc. Fig. 2 is the small signal model of frequency compensation for Fig. 1.

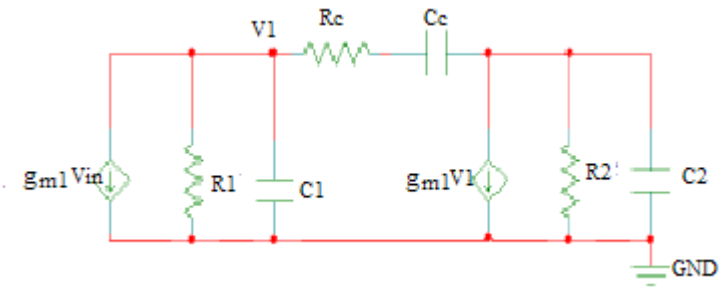

Fig.2 the small signal model of frequency compensation

Assuming Rc=0, using the node current analysis way, we can get:

$$\begin{aligned} g_{m1}V_{m1} + V_1 \cdot (\frac{1}{R_1} + sC_1) + (V_1 - V_{out}) \cdot sC_c = 0 \\ g_{m6}V_1 + V_{out} \cdot (\frac{1}{R_2} + sC_2) + (V_{out} - V_1) \cdot sC_c = 0 \end{aligned} \tag{7}$$

The following equation can be obtained by the above equations combined solution:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m6}R_1R_2(1-\frac{sC_c}{g_{m6}})}{a_2s^2 + a_1s + 1} \tag{8}$$

In middle :

$$\begin{aligned} a_2 &= R_1R_2(C_1C_2 + C_1C_c + C_2C_c) \\ a_1 &= (C_1 + C_c)R_2 + g_{m6}R_1R_2C_c \end{aligned} \tag{9}$$

In the actual circuit, the two poles are very far apart, $w_{p2} >> w_{p1}$

$$H(s) = (1-\frac{s}{w_{p1}})(1-\frac{s}{w_{p2}}) = 1 - \frac{s}{w_{p1}} + \frac{s^2}{w_{p1}w_{p2}} \tag{10}$$

So, $$\frac{1}{C_c(\frac{1}{g_{m6}} - R_c)} = \frac{-g_{m6}}{C_1 + C_2} \tag{11}$$

The value of Rc is： $$R_c = \frac{1}{g_{m6}}(1 + \frac{C_1 + C_2}{C_c}) \tag{12}$$

We can get

$$g_{m6}C_c^2 > g_{m1}C_1C_2 + g_{m1}C_1C_c + g_{m1}C_1^2 > g_{m1}C_1C_2 \tag{13}$$

And $$C_c > \sqrt{\frac{g_{m1}C_1C_2}{g_{m6}}} \tag{14}$$

We use the Spice to simulation the Op, and it is based on standard 0.18um CMOS technology, with 3.3 power supply.

3. Analysis of Result:

The Fig 3 has showed that the amplifier DC gain is 106db, the gain-bandwidth is 167MHZ, and the phase margin is 75^o. Table1 has given the measured performance, the simulation showed the ADC can achieve 8bits resolution and 10Msamples/s.

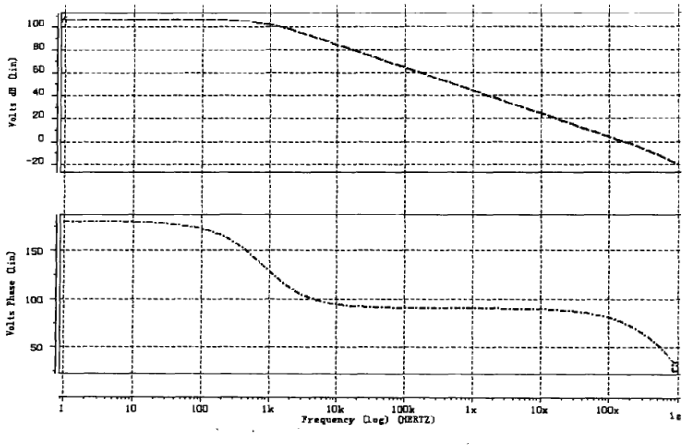

Fig.3 the performance of 8 Bits Pipeline ADC

Table 1 Measured Performance

Supply voltage	3.3V
Load capacitance	3 pf
Common in-put voltage	1.65V
Output Dynamic Range	[0.33V, 2.97V]
Open-loop DC gain	106 db
Phase margin	75^0
Conversion rate	35V/us

4. Conclusion

Analog-to-digital conversion can be accomplished in numerous ways, but apart from flash converters, only pipeline of analog-to-digital conversion (ADC) are well known for producing accurate, medium speed conversion of analog signals. The 8 bit pipeline ADC was proposed for low-power low-cost CMOS integrated system. The experimental results showed that the proposed circuits achieves 10Ms/s sample with power consumption at 3.3V. This device is suitable for standard CMOS technology VLSI implementation. It is well applied when embedded into system-on-chip (SoC) circuit designs.

Acknowledgements

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