

## Diagnosis Method Based on Chaos Optimization Algorithm of The Testability of Complex circuit system

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**Abstract.** It needs to put structure of boundary scan in the circuit board for improving the controllability and observability of the device in complex circuit board. At the same time when structure of boundary scan improves pcb-level circuit testability, it also increased the complexity of circuit design which needs to weigh the testability improvement and design complexity, two factors. In view of the combinatorial optimization problem of the design complexity and minimize, solving method based on chaos optimization algorithm is proposed. Through example validation, the algorithm were obtained good results on optimization effect and operation time. The fact proved that, the algorithm can be effectively applied in board-level circuit testability design optimization and improving pcb-level circuit testability.

### I Introduction

The emergence and development of the Very large scale integrated circuit (VLSI), Surface mount devices (SMD), Multilayer printed board (MPCB) make the test in the face of board-level circuit nodes of physical accessibility gradually weakened, and the board level circuit testability fell sharply. To solve the problem of board-level circuit test, the European Joint Test Action Group puts forward Boundary Scan Technique, Boundary scan test is a test for board test design method, it by boundary scan unit to complete the test devices and peripheral circuit, greatly improving the controllability and observability of the device.

But at the same time with the additional design of the structure in order to improve the circuit testability design of boundary scan, it also increases the complexity of circuit board design. Therefore, it needs to weigh the testability improvement in the design of circuit board and design complexity, two factors to improve the testability of board-level circuit design. At present, common practice is to simplify the problem into two sub-problems, one is when the testability improvement is fixed, how to minimize the complexity of design trade-off design, the second is when the design complexity is fixed, how to weigh the design to maximize testability improvement[1][2].

This paper, by using chaos optimization algorithm to solve the combinatorial optimization problem, the algorithm takes advantage of the characteristics that the chaos phenomenon can not repeat iterates through all status of the system, not only it is a global optimization algorithm, it also has faster convergence speed, it can be effectively applied to solve combinatorial optimization problems.

### II Mathematical description of the problem

In the case of symmetric test hypothesis, the traditional signed digraph model based fault diagnosis problem can be described in a quad, like  $\langle S, T, P, D \rangle$ , which includes,

(1) Underlying the cause of the problem sets  $S = \{s_1, s_2, \dots, s_m\}$

(2) Binary output available test set  $T = \{t_1, t_2, \dots, t_n\}$

(3) With prior probability of fault source correlation set  $\underline{p}(S) = \{p(s_1), \dots, p(s_n)\}^T$

(4) Rely on matrix  $D = [d_{ij}]_{(m \times n)}$

Where, in each test  $t_j, 1 \leq j \leq n$ , is the  $j$  column of the matrix:  $\underline{d}_j = [d_{1j}, d_{2j}, \dots, d_{mj}]^T$ , which provides if  $t_j$  can test  $s_i$ ,  $d_{ij} = 1$  or  $d_{ij} = 0$ .

Let each test correspond  $m$  class outputs, ( $m = 2$  when Binary output), it can maximum constitute  $f(m, |T|)$  test sequences, where,

$$f(m, |T|) = m^{|T|} |T|! \quad (1)$$

Let can build  $g(m, |T|)$  test trees most, there is

$$g(m, |T|) = \begin{cases} 1 & m > 0, |T| = 1 \\ m^{|T|-2} |T|! & m > 0, |T| > 1 \end{cases} \quad (2)$$

If you want fault fuzzy set of the elements in the less than  $d$ , it can constitute  $h(|S|, d)$  fault fuzzy groups, where,

$$h(|S|, d) = 1 + \sum_{i=1}^d \binom{|S|}{d} \quad d \leq |S| \quad (3)$$

When the design of fault isolation strategy,  $S$  is divided into two subsets: set  $H$  which may be cause the problem and set  $G$  may not be cause the problem. Make  $G_i$  and  $H_i$  respectively the problem sets which are possible or not possible when perform after  $i$  tests.  $G_i$  and  $H_i$  respectively the possible or not possible cause of the problem sets during  $i$  test, where,

$$H \cap G = H_i \cap G_i = H^l \cap G^l = \Phi \quad (4)$$

$$H \cup G = H_i \cup G_i = H^l \cup G^l = S \quad (5)$$

$$Z_{2n} = 0.17 \quad (6)$$

In the initial stages of the isolation of malfunctions, as well as no testing started.  $H^0 = F$ ,  $G^0 = \Phi$ . The generation of malfunction isolation will convert into the problem of congregation dipartition in the progress of testing picking.

#### A Boundary scan based board-level testing of the design and implementation of technology

We usually use two methods as below to put boundary scanning circuit into circuit board with JTAG[2][3]:

(1) Boundary scan devices Replacement

Boundary Scan device replacement method refer to selecting the device with Boundary-Scan Architecture and same function to replace the original non-boundary scan devices, during design board-level testability, so that it contains boundary scan structure to achieve board-level information controllability and observability.

(2) Embed Boundary-Scan Architecture

Embed Boundary-Scan Architecture is the method of putting boundary-scan register structure directly into the functional circuit, which boundary-scan device can utilize its own boundary scan cells to achieve the controllability and observability of non-boundary scan devices.

#### B Optimization analysis of Board-level testability Design

In the above two methods to improve the using of board-level testing, due to increased additional circuitry with boundary scan structures, which also increases the circuit board design complexity. Therefore, we generally analyze the problem from two aspects: one is edure testability is improved, how to make design complexity to the least; the second is a certain complexity of the design, how to make the most improved testability.

This paper studies the issue of design complexity minimization. Because there is a certain relationship between the interconnection device pins, when tested at the disposal of the interconnect pin into a boundary-scan architecture can be achieved with a series of pin control and observation. Thus, the candidate placed point Boundary-Scan Architecture focuses on minimal devices, placed a minimum of boundary-scan devices. Therefore, while enduring improved testability, the problem of making the complexity of the design to minimize can be described as: Looking for the minimum number, and covers all the tests of the device design criteria established set of interconnections.

Supposing qualitatively select  $l$  points on circuit boards into boundary scan architecture, which separately belonging  $n$  devices  $U = \{u_1, u_2, \dots, u_n\}$ , and  $m$  is an interconnect circuit network  $V = \{v_1, v_2, \dots, v_m\}$ , if arbitrarily selecting point in each network, it will meet the completeness requirements of test. Therefore, the design complexity minimization problem can be described as: Looking for the columns device of minimum number, so that it covers all of the pins of circuit network. The problem can be described with a matrix A, the rows  $m$  of matrix is the number of the network, the number  $n$  is the number of columns of the device, the  $i$ -th row and  $j$ -th element of A is defined as:

$$a_{ij} = \begin{cases} 0, u_i \text{ and } v_j \text{ have collect relationship} \\ 1, u_i \text{ and } v_j \text{ don't have collect relationship} \end{cases}$$

Therefore, the goal of optimizing the algorithm is to get the smallest number to device to cover all network.

### III Chaos theory and optimization algorithm

#### A Characteristics of chaotic motion

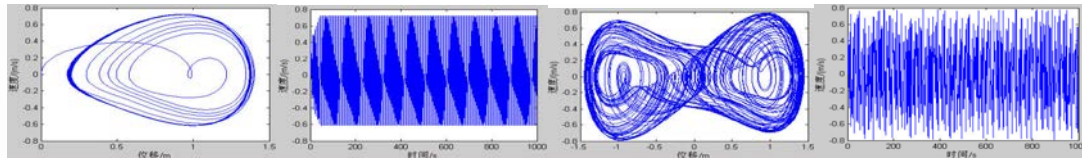
By means of Duffing oscillator, the chaotic state of the system can be obtained by the Duffing equation. The nonlinear system has been proved to be a chaotic system. As shown in formula (1)[4]:

$$\begin{aligned} \dot{x} &= \omega y \\ \dot{y} &= \omega(-cy + x - x^3 + F \cos(\omega t)) \end{aligned} \quad (1)$$

Where, the  $\dot{x}$  and  $x$  are the state variables,  $F \cos(\omega t)$  is a periodic driving force,  $c$  is the damping ratio,  $-X + X^3$  is the nonlinear restoring force,  $\omega$  is the driving force angle frequency;  $F$  is the periodic driving force amplitude.

The system state has a strong sensitivity to the amplitude  $F$ , and the amplitude  $F$  is different, and the solution of the system presents different states in the phase space. When the  $c$  fixed, regulation  $F$  increases gradually from 0, system solutions in the phase space according to the applied force cycle cycle small scale periodic oscillation; when  $F$  increases to a critical value of  $F_1$ , then it appeared homoclinic orbits and chaotic, when  $F$  increases more than threshold  $F_2$  system changed from chaotic motion for according to the applied force period of large-scale periodic oscillation. That is to say, when the  $F$  changes, the system is converted to three kinds of states in the period of the system in the period 1 inner rail movement, the chaotic motion, the period 1 outer rail movement.

In this paper, we take  $c = 0.5$ ,  $\omega = 1 \text{ rad/s}$ , step  $\Delta t = 0.1 \text{ s}$ , the motion trajectory of the duffing oscillator is obtained as shown in Figure 1.  $F_1$  is between 0.38~0.39.  $F_2$  is between 0.82~0.83.



(a) period 1 inner rail (b) chaotic motion

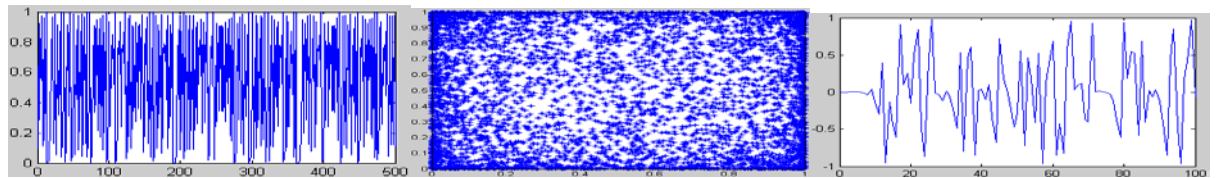
Figure 1 Motion trajectory of Duffing oscillator

Figure 1 (b) is a state of motion which is obtained by the Deffing equation, which is called the chaotic motion state, and the variable is called the chaotic state. Logistic. Mapping is a typical chaotic system, As shown in formula (2)[5]:

$$z_{n+1} = u \cdot z_n(1 - z_n) \quad (n = 0, 1, 2, \dots) \quad (2)$$

$0 < z_n < 1$ , when  $\mu = 4$ , The system is a full mapping of the  $[0, 1]$  interval, showing a complete chaos state. The characteristics of the chaotic motion state are described.

When the initial value of  $Z_0 = 0.1$ , according to equation (2) chaotic trajectories obtained in Figure 2 (a) shows, it can be seen from the figure, the chaotic motion is random; take the initial value of  $N$ ,  $Z_{20} = 0.1158$ , according to equation (2) can obtain two chaotic trajectory, respectively by  $Z_{1n}$  and  $Z_{2n}$  as the horizontal and vertical coordinates, then obtain Figure 2 (b), it can be seen from the figure that with the increase of the number of chaos variables continue all states will traverse the system, the initial value of  $Z_{10} = 0.1157$ ,  $Z_{20} = 0.1158$ , according to equation (2) to obtain two chaotic trajectory respectively, with the difference between the two variables as the ordinate, with variable iteration curve 2 (c), it can be seen from the figure, although the difference of the two initial chaotic variables is very small, but with the continuous change of variables, the two will be a big difference, so it can be known that the chaotic motion state is very sensitive to the initial value.



(a) randomness (b) ergodic (c) sensitivity of Initial value

Fig.2 Plot of The characteristics of chaotic motion

## B Chaos Optimization Algorithm

Basing on the characteristics of the chaotic motion, Li bing[6]put forward the Chaos Optimization Algorithm, this algorithm uses method of similar carrier to introduce the chaotic state into the optimization variables, and enlarged scope of chaotic motion of traverse to the scope of optimization variables and then using the chaotic variables to search. The chaotic variables which used as carrier usually uses the Logistic mapping like formula (2).

For optimization problems of a class of continuous objects:

The basic steps of the algorithm are as follows:

Step 1: Using the characteristics that chaotic state is sensitive to initial value, giving formula (2) has  $m$  tiny difference of initial values ( $m$  is the number of variables in optimization problems),  $m$  different trajectories of chaotic variables  $z_{i,n+1} (i = 1, 2, \dots, m)$  can be obtained.

Step 2: Using the carrier expression like formula (4), mapping chaotic variables to optimize variable scope.

$$x_{i,n+1} = c_i + d_i \times z_{i,l+1} \quad (4)$$

Where,  $c_i = a_i$ ,  $d_i = b_i - a_i$ .

Step 3: Chaotic searching. Let  $x_i(k) = x_{i,n+1}$  and solve  $f(x_i(k)) \leq$ . When  $k = 1$ , let the optimal value of a function  $K = k + 1$ , the value of optimal variables is  $x_{best} = x_i(1)$ , and then

search as follows:

$$\begin{aligned}
 & \text{if } f(x_i(k)) \leq f_{best} \\
 & f_{best} = f(x_i(k)); \\
 & X_{best} = X_i(k); \\
 & \text{end} \\
 & K = k + 1;
 \end{aligned}$$

Step 4: If after the step after several iterations  $f_{best}$  remains the same, the value could be the optimal solution.

#### IV the Minimize optimized solving of design complexity based on COA

Applying COA to board-level circuit complexity minimization problem solving, considering the adaptability of the algorithm, it needs mainly to solve the following problems:

Binary code

Due to the design complexity minimization problem can be described in matrix, therefore, the chaos variables with binary coding, the total number of variable dimension for the device  $N$ , each dimension has a value of 0 or 1, when it is 0, it means don't choose the device; when it is 1, it means choose the device.

Constructing the fitness function

Based on the above analysis of design complexity minimization problem, the constructed fitness function is:

$$\begin{aligned}
 f &= \min \sum_{i=1}^N a_i \\
 s.t. \quad & \forall a_{diag}(j) \in \text{Diag}(S_A \times S_A^T) \neq 0 (j = 1, 2, \dots, M)
 \end{aligned} \tag{6}$$

Where,  $S_A$  is the choice of the corresponding matrix of particles,  $\text{Diag}$  is mean to take on the diagonal matrix elements,  $N$  is the total for the device,  $M$  is as the total number of circuit network.

The constraint condition of the fitness function is to cover all of the network, which means the testability improvement is fixed, the objective function is to select the minimum number of device.

#### V Verify

Assuming that the boundary scan candidate in points after simplified processing of the circuit board are 81, affiliated to 8 devices  $U = \{u_1, u_2, \dots, u_8\}$ , and then connecting to 35 networks  $V = \{v_1, v_2, \dots, v_{35}\}$ , the specific subordinate relations are:

- u1:  $\{v_1, v_2, \dots, v_{16}\}$ ;
- u2:  $\{v_1, v_6, v_{10}, v_{11}, v_{17}, v_{18}, v_{20}, v_{21}, v_{24}, v_{27}, v_{29}, v_{31}, v_{32}, v_{34}\}$ ;
- u3:  $\{v_2, v_7, v_{14}, v_{17}, v_{20}, v_{24}, v_{35}\}$ ;
- u4:  $\{v_4, v_{15}, v_{18}, v_{20}, v_{21}, v_{23}, v_{24}, v_{26}, v_{28}, v_{30}, v_{33}, v_{34}\}$ ;
- u5:  $\{v_5, v_{10}, v_{16}, v_{18}, v_{24}, v_{29}\}$ ;
- u6:  $\{v_7, v_{12}, v_{19}, v_{22}, v_{23}, v_{25}, v_{26}, v_{28}, v_{30}, v_{33}, v_{35}\}$ ;
- u7:  $\{v_8, v_9, v_{17}, v_{19}, v_{22}, v_{25}, v_{27}, v_{35}\}$ ;
- u8:  $\{v_3, v_9, v_{13}, v_{20}, v_{21}, v_{27}, v_{31}\}$ .

Through debugging and running in MATLAB software, the optimization result is  $\{v_1, v_2, v_6\}$ , the relation curve between the best fitness value and the number of iterations is shown as picture 3. From the picture we can see that when iteration to about 10 times, COA algorithm can search the optimal solution, the total run time for program is 1.4840s, and the time to search the optimal solution is 0.15s, it has greatly improved in time compared with the graph algorithm, the data are

shown in table 1.

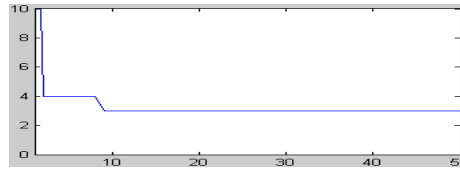


Fig. 3 Plot of the best fitness value curve of COA algorithm

Table. 1 Comparison of three kinds of algorithm optimization results

Types of algorithms	optimization results	Running time (s)
greedy algorithm	u1, u2, u4, u7	$4 \times 10^{-6}$
graph algorithm	u1, u2, u6	56.7
Chaos optimization algorithm	u1, u2, u6	0.15

## VI Conclusion

This paper studied board level testability design optimization method, at the same time that set boundary scan structure in circuit board to improve its test, it also Increased the complexity of the circuit board design, it needs to weigh the testability improvement and design complexity, two factors. Design complexity minimization problem is studied in this paper, and optimization method based on COA algorithm is proposed, comprising with greedy algorithm and graph algorithm, the algorithm is proved to improve the effectiveness of board-level testability design.

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