Design and Realization of FPGA Based Phonetic Intelligent Home System

Wei Zhuo

Vocational Education Department, Liaoning Police College, Dalian, 116036, China

Email：1567757@qq.com

Keywords: voice recognition; FPGA; intelligent home

Abstract: This paper aims at designing a set of FPGA based phonetic intelligent home system, wherein this system completely adopts wireless communication technology to avoid rewiring problem and can control home appliances through voice recognition and infrared sensor, thus to phonetically turn on or turn off lighting lamp, air conditioner, TV set, refrigerator, etc. in a real-time manner. Meanwhile, the hardware and software design and the structure principle of the system are specifically explained in this article. The experimental verification shows that voice recognition technology has a wide application prospect in intelligent home systems.

Introduction

Along with the improvement of intelligent life level, intelligent home products are gradually integrated with the daily life of thousands of families. For example, such home appliance manufacturers as Gree and Tsinghua Tongfang have correspondingly designed different intelligent home products. At present, the control and management commands of most intelligent home systems are mainly composed of a few of specific word groups and numeric strings, so it is feasible and realizable to apply the conjunction voice recognition systems in intelligent homes. Moreover, the application of non-specific voice recognition technology is also significant for intelligent homes. In a word, voice control can significantly improve the convenience of intelligent home.

Voice Recognition Technology Principle and Composition

Voice recognition technology [1] includes two basic steps, wherein the first step is system “learning” or “training”, and mainly aims at establishing acoustic model and grammar analysis language model; the second step is “recognition” or “testing”, and mainly aims at selecting a suitable recognition method according to the type of the recognized system and meanwhile adopting corresponding voice analysis method to extract phonetic features needed by this recognition method in order to judge and obtain the recognition result through comparing these features with the system model according to relevant standards and measurement [2] . The realization process of a typical voice recognition system is as shown in Fig. 1.

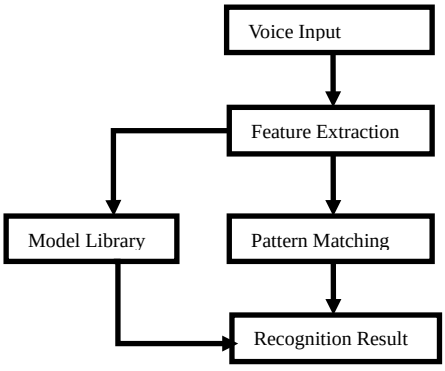

Fig.1 Realization Process of Voice Recognition System

Embedded IP Hardcore SOPC System Based on FPGA

This idea namely refers to the transplantation of a microprocessor into FPGA. Specifically, the present popular 32bit ARM intellectual property processor is transplanted into FPGA through a hardcore form, then the rich logical resources and IP soft cores in FGPA are made into interface function modules to configure SRAM, SDRAM, FLASH drives, etc., and network communication interface, UART, USB, view screen interface, audio acquisition, keyboard interface, SPI, communication interface, etc., thus to solve the system integration problem and meanwhile improve the overall performance and reduce power consumption, etc. Moreover, such companies as Altera and Xilinx have also correspondingly promoted the transplantation of ARM920T processor core into FPGA in order to improve the performance of SOPC system and accordingly organically integrate the hardware design customization of FPGA and the strong software function of the embedded microprocessor [3]. In this system, we adopt the embedded system microprocessor IP soft core of Altera Nios soft core 32bit/16bit bus instruction set and data channel, and meanwhile take Quartus II software development platform as SOPC carrier, so developers can flexibly configure multiple user interface modules such as Cache, RS232, SDRAM controller, tristate bridge, standard Ethernet interface, DMA, timer able to generate Baud rate, multiple co-processors in Avalon bus through Nios II core generated by Qsys, thus to realize dual CPU and multi-core co-processors for multi-computer communication. Meanwhile, the soft core can be directly exported according to the guideline, namely generating a scalable user CPU. As for the cost, Nios is a non-third party intellectual property directly promoted by Altera, so users may not pay the intellectual property cost, which is also an important factor considered thereby during design and development process.

For digital signal processing, Matlab is a necessary system analysis and simulation tool for us [4]. Meanwhile, as a plug-in of Matlab, DSP Builder is integrated with Matlab to enable users to directly adopt Simulink in Matlab to complete the system-level design, and Altera Corporation also provides rich IP modules conveniently for users to call. Additionally, developers have integrated the modules generated by DSP Builder into Quartus II in order to generate Vhdl language and unit top module, thus to be combined with Nios II to realize in-chip embedded system.

System Hardware Design

Hardware development platform: the hardware platform of this system is established on Storm_IV_E6_V1.0 development board platform of Hengxing Science & Technology Co., Ltd, with the core controller as Cyclone IV EP4CE6E22C8 chip. All important components are connected on the core control chip, so designers can control various functional components through programming [5].

24bit audio coder: high-quality 24bit Wolfson WM8731 coding and decoding chip is adopted. The chip has three ports respectively for microphone input, wire input and wire output, with the sampling frequency adjustable between 8KHz and 96KHz, and transmits data through fixed I2C bus protocol. The specific realization diagram is as shown in Fig. 2.

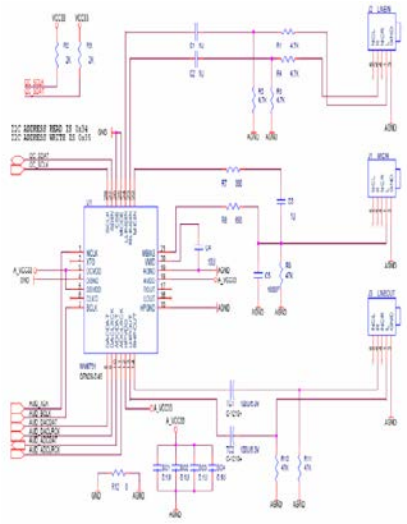

Fig. 2 Hardware CircuitFig

Memory circuit: we select 256K*16bit high-speed asynchronous SRAM for the memory circuit, and the power voltage is selected as 3.3V, and the data width is from low 8bit to high 8bit. Reading and writing operations are carried out according to the time sequence requirement of the chip. Additionally, we divide the memory into 5 areas, wherein the first area is used to access the continuous voice messages collected thereby (specifically reading 3 isolated words at one time) and the last three areas are used to store three effective voice segments of breakpoint detection.

Human-machine exchange part: we adopt 16X2 1206 LCD module as the human-machine exchange interface to display prompt information.

The specific realization circuit is as shown in Fig. 3.

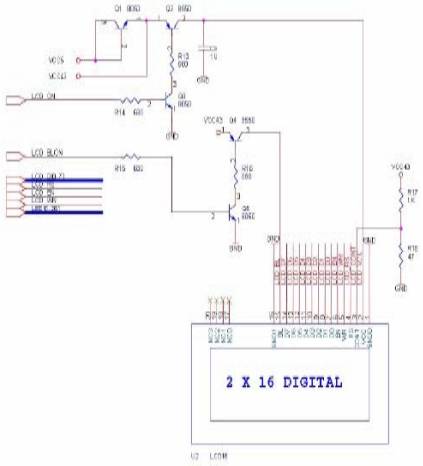

Fig. 3 LCD Control Circuit

External control circuit of intelligent home: we adopt infrared emitter to respectively control cable TV set, air conditioner, desk lamp, monitoring camera, etc. through following language instructions: “Jiajia” please activates the host computer; then the host computer answers: “master, what can I do for you?”, and then the user can “turn on the lamp”, “turn off the lamp”, “turn on the air conditioner”, “turn off the air conditioner”, “turn on TV set” and “turn off TV set”. Meanwhile, the user can further control home appliances through voice instructions: for example, use such voice instructions as “switch to CCTV 1” and “switch to LNTV” to switch TV channels; use such voice instructions as “turn left”, “turn right”, “turn upward” and “turn downward” to control the activated monitoring camera.

System Software Design

After being powered on for initialization, the system enters voice recognition system, wherein the high-speed voice signal processing unit includes: voice endpoint detection module and phonetic feature extraction module; the voice detection module as the core module has FIR filter design and

can calculate energy and zero-crossing rate; the voice extraction & processing unit includes base-2256 FIR module, MEL filter bank, DCT discrete cosine transform module, etc. Moreover, DTW recognition algorithm is applied for the recognition unit, and the above processing function units are designed into IP CORE through Verilog HDL in order to apply Pipline and ping-pong operations to realize data telling processing. Above IP CORE data exchange employs bus transmission and Nios II control to realize data DMA operation, without the intervention of CPU, thus to maximally improve the operating speed.

Main algorithm flow is as follows in Fig. 4.

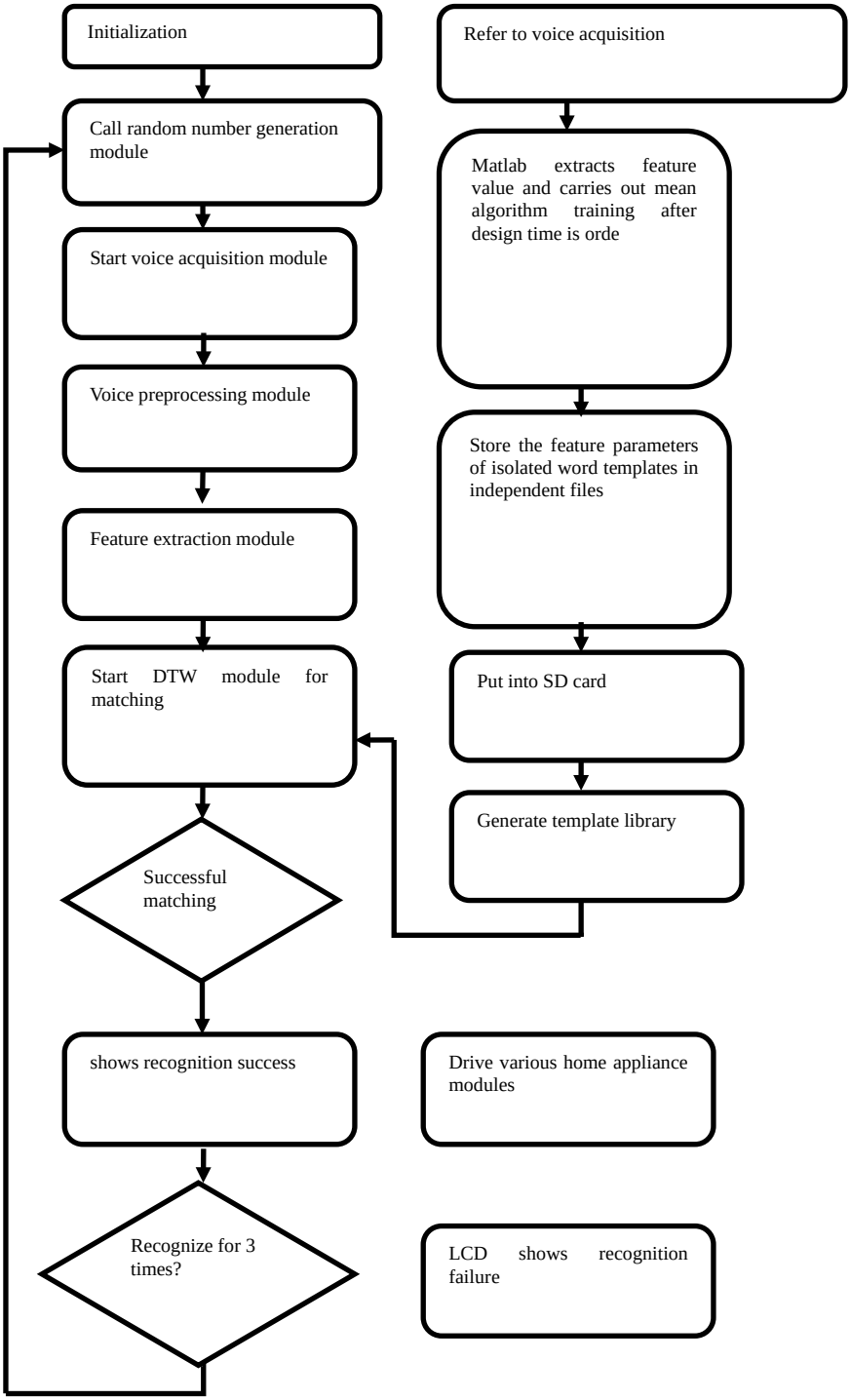

Fig. 4 Algorithm Flow Chart

System Test

This voice recognition system of intelligent home employs non-assigned person voice recognition to control the home appliances through intelligent home system, and the key point for the success of the system lies in the success rate of recognizing different voices [6] [7] . After hardware and software of the system are well designed, it is necessary to download the control codes of the phonetic intelligent home to FPGA core chip in order to phonetically train the whole system and further adopt the voice recognition system to control home appliances after phonetic training.

Take voice control over cable TV set as an example: firstly, the user says: “Jiajia”, then the host computer answers: “master, what can I do for you?”, then user says: “ please turn on TV set”, then the host computer replies: “it will be ok at once”, then the TV set is turned on; afterwards, the user can adopt similar voice instructions in above two steps to switch TV channels, turn off the TV set, etc. Similarly, other home appliances can be controlled through such voice instructions [8].

The accents of different provinces are divided into A, B, C and D groups for the phonetic test of the system, wherein the success rates of one-time voice instruction realization operations are respectively 91%, 90%, 94% and 96%, and the success rates of three-time voice instruction realization operations can reach 99%.

The actual test result shows that the intelligent home voice recognition system has relatively high voice recognition capability and extremely high stability, and can correctly recognize different mandarin accents and properly execute corresponding operations [9]. Therefore, this voice recognition system can be well applied to the control systems of intelligent homes.

Conclusion

This article aims at introducing the intelligent home voice recognition system with FPGA as the core and respectively explaining SOPC design, Nios II core development design, voice recognition principle and realization framework, hardware design of voice recognition unit, external hardware circuit design, system software design, etc. The experimental result shows that voice recognition technology has wide application prospect in intelligent home products and this system proposed thereby can be expanded into more complicated intelligent home system. In a word, this intelligent home voice recognition system is suitable for people at all ages and can be operated by non-assigned persons, so it has wide market prospect.

Acknowledgements

This work was supported by science fund education office of liaoning province (NO. L2014511) .

References:

[1]Wang Fuzhong, Huang Wenhao, Intelligent Control System Design Based on Voice Recognition Technology [J], Automation and Instrument, 2006, 21 (4) : 8-10.

[2]Luo Zhizeng, Zhao Jingbin, Robot Voice Control and Realization [J], Journal of Hangzhou Institute of Electronic Engineering, 2004, 24 (1): 30-34.

[3]Institute of Electrical and Electronics Engineers, Inc. IEEE Standard for Information Technology-Telecommunications and Information Exchange between Systems-Local and Metro Politan Area Networks-Specification Requirements-Part 15.4: Wireless Medium Access Control (MAC) and physical Layer (PHY) Specifications for. IEEE Std 802.15.4-2003

[4]Akyildiz IF, Su W, Sankarasubramaniam Y, Cayirci E. Wireless sensor networks: a survey. Computer Networks . 2002

[5]Charles E Perkins, Elizabeth M Royer, Samir R Das. Ad hocon-demand distance vector routing. RFC 3561 . 2003

[6]Anand Ranganathan, Robert E Mcgrath, Roy H Campbell, M Dennis Mickunas. Use of ontologies in a pervasive computing environment. The Knowledge Engineering Review . 2003

[7]Naoharu Yamada, Kenji Sakamoto, Goro Kunito, Yoshinori Isoda, Kenichi Yamazaki, Satoshi Tanaka. Applying Ontology and Probabilistic Model to Human Activity Recognition from Surrounding Things. IPSJ Digital Courier . 2007

[8]Bonner S.Education in ancient Rome: From the elder Cato to the younger Pliny . 2011

[9]Tsarkov D, Riazanov A, Bechhofer S, et al.Using Vampire to reason with OWL. TheSemantic Web – ISWC2004 . 2004