A 5-Gb/s 156-mW Transceiver with FFE/Analog Equalizer in 90-nm CMOS Technology

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Abstract. A 5-Gb/s transceiver in 90nm technology has been presented in this paper. To mitigate the effects of channel loss, a 4-tap feed-forward equalizer (FFE) is included in the transmitter. Meanwhile, the receiver employs continuous-time linear equalizer (CTLE) to amplify high frequency signal. The clocks of the transmitter are supplied by Phase-Locked Loops (PLL) while clocks in the receiver are provided by clock recover circuit (CDR). To facilitate the testing, built-in pseudo-random sequence (PRBS) generator and PRBS detector are integrated in this chip. Fabricated in 90nm CMOS technology, the transceiver consumes 156mW under 1.2V supply.

Introduction

With the rapid development of wire-line communication, data rates grow exponentially over the past decades, especially in digital computing and signal processing fields. In order to meet the growing demand for high-speed data transmission, Serdes (Serializer/Deserializer) is gradually replacing the traditional parallel buses and becoming the mainstream of high-speed interface. Serdes is a kind of multiplexing technology that converts data from parallel to serial, reducing the communication channels and chip pins.

In inter-chip communication over PCB or backplane, avoiding reflection and Inter-Symbol Interference (ISI) are the main challenges for robust communication. Reflection in transmission line (T-line) can be reduced by proper T-line design. But ISI stems from Low-Pass Filter (LPF) characteristics of the actual line and becomes severe as either the data rate or the length of the T-line increases. Hence, ISI compensation is critical in over 5-Gb/s data communication. Equalizers in transmitter and receiver are necessary for compensation of ISI.

This paper describes the design of key elements of a 5-Gb/s transceiver. The transceiver uses fixed transmitter feed-forward equalizer (FFE) in combination with analog equalizer in the receiver for line equalization. A system design overview including a description of FFE, analog equalizer and the transceiver architecture will be given. Next, the key circuit components of the transceiver will be described in detail. These components include the FFE-based transmitter equalizer, a linear receiver analog front-end with Continuous-Time Linear Equalizer (CTLE), Limiting Amplify (LA) and Slicer.

Fabricated in 90-nm CMOS technology, the transceiver dissipates 156mW from a 1.2V supply and Phase-Locked Loops (PLL) is integrated on chip in this paper.

Structure of Transceiver

The transceiver architecture is shown in Fig.1. The transmitter is composed of 8:1 multiplexer (MUX) and pre-emphasized circuit. The transmitter FFE has programmable tap settings that are normally set to fixed values. The receiver includes analog equalizer, slicer and 1:8 demultiplexer (DEMUX). The receiver implements asynchronous local clock recovery using off-chip clock recover circuit (CDR). The 50-Ω single-end line terminations may be ac or dc coupled to the external line. The transmitter dissipates 72mW and produces an amplitude of 550 mV peak-to-peak differential (mVppd) into a 100-Ω differential load.
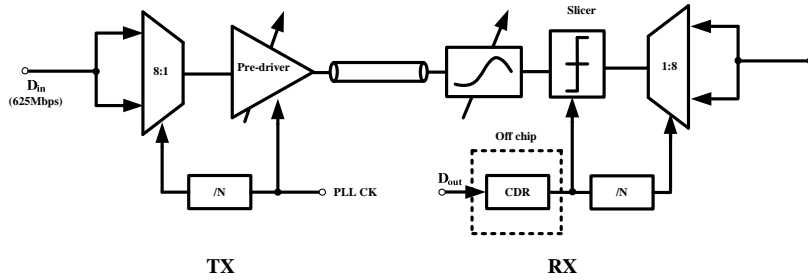
Fig.1. Transceiver architecture

Structure of Transmitter

The complete transmitter architecture is shown in Fig.2 [1] [2]. To facilitate the testing, a built-in 2^7-1 (pseudo-random sequence) PRBS generator is included to provide eight 625Mbps pseudo-random inputs for the 4:1 MUX stage. The blocks of 4:1 MUX and 2:1 MUX serialize the input data into 5Gbps. Like many other mainstream designs, FFE is employed. However, the number of taps for FFE should be considered. We stimulate the response of different FFEs having 2, 3 and 4 taps. As a result, the FFE with 4 taps exhibits sufficient gain in high frequency. The Fig.3 illustrates the response of FFE having 4 taps. Another issue is the parasitic capacitance caused by the taps. Adding more taps implies linear increase of parasitic capacitance at the output node. Since bandwidth is inversely proportional to this capacitance. Thus, in this design, we choose 4 taps as a compromise between bandwidth and accuracy. The PLL is responsible for multiplying a reference clock by 40, providing 5GHz clock for the transmitter.
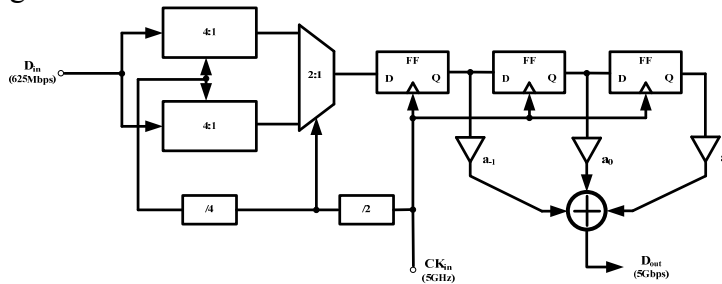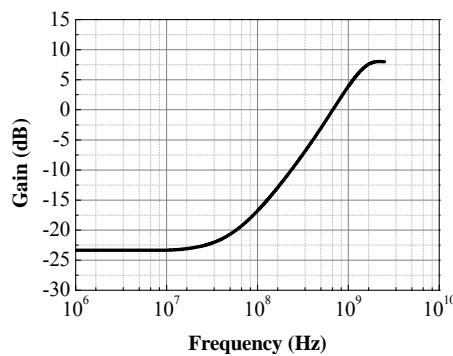

Fig.2. Transmitter architecture

Fig.3. Transfer function of pre-driver

A. FFE

The FFE structure is shown in Fig.4. The data streams are shifted by in unit interval (UI) for the first tap of FFE. Additional shifting yield the delayed data for the remaining 3 taps of the FFE. After sign selection, the output of these currents are summed together in the line termination loads. The FFE taps have been sized to maximum relative weights of 0.25, 1.0, 0.5, and 0.25(with one pre-cursor and two post-cursors) [3]. Fig.5 demonstrates simple model of FFE. The tap weights are programmed by means of controlling the tail currents.

Fig.4. FFE structure

Fig.5. Simple model of FFE

B. MUX

The MUX design is shown in Fig.6. With the help of rail-to-rail clock, the selection of the two streams is accomplished. The block serializes the data into 5-Gb/s. This block involves tradeoff between gain and bandwidth. The MUX must exhibit high gain to provide sufficiently voltage swing for subsequent block while the circuit bandwidth must maintain 2.5GHz. The MUX is composed of Current-Mode-Logic (CML) circuits and thus restore the output signal back to CML levels.

Fig.6. MUX

Structure of Receiver

Fig.7 shows the receiver architecture. A built-in PRBS detector is also integrated in the chip to detect the output of 1:8 DEMUX. In the receiver, ISI compensation is critical in over 5-Gb/s data communication. Fortunately, CTLE [4] provides high-frequency boosting to compensate the low-pass effects of non-ideal channel while providing 50Ω termination. LA follows CTLE in the front end to provide sufficiently large voltage swings for the subsequent Slicer. In order to retime data, Slicer is employed subsequently. At last, 1:8 DEMUX deserializes high speed data into 625Mbps.

Fig.7. Receiver architecture

A. CTLE

ISI compensation is critical in over 5-Gb/s data communication. One approach to implement equalization is to use CTLE that provides gain peaking in order to boost up high-frequency to compensate attenuation. The main advantages of this approach are lower power, less silicon area.

The CTLE scheme is shown in Fig.8. Peaking frequency is designed not to lower 2.5GHz for 5-Gb/s signaling. If peaking is lower than 2.5GHz, lower frequency components such as 1.5GHz component are more emphasized compared to 2.5GHz, then 2.5GHz is suppressed by 1.5GHz signal and failure of equalization occurs. Peaking magnitude of CTLE is designed to range from 6dB to 8dB by 2b switch.
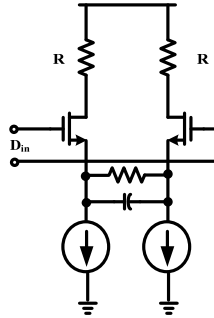
Fig.8. CTLE

B. LA

The LA design is depicted in Fig.9 [5]. As the intermediate stage between CTLE and Slicer, the LA must satisfy a number of requirements. Firstly, the LA must exhibit high gain to provide sufficiently large voltage swings for the subsequent Slicer. Moreover, the circuit bandwidth must approach 2.5GHz to avoid ISI.

The LA offset may also impact the receiver performance. Vertical shift of the signal with respect to the decision threshold will degrade the receiver sensitivity.

The architecture consists of three identical gain stages comprising the LA core, an offset cancellation feedback loop and an output buffer. (1) The LA core must provide sufficiently large gain and bandwidth; (2) continuous-time offset cancellation circuits introduce a lower cutoff frequency in the transfer function.

The LA core is constituted by 3 stages CML. Suppose the gain of every stage is A, we can write the closed loop transfer function:

$$F(s) = \frac{A^3 \square (1 + sRC)}{A^3 + 1 + sRC} \tag{1}$$

At the low frequency, the function will yield:

$$F(s) \approx \frac{A^3}{A^3 + 1} \tag{2}$$

Fig.10 depicts the response of LA and shows that the LA core has provide sufficiently large gain and the dc offset will be attenuated.
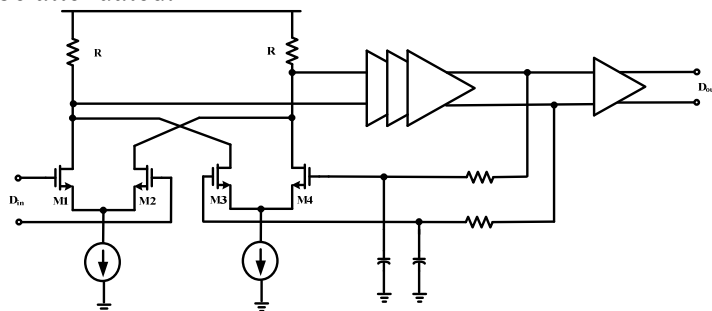

Fig.9. LA
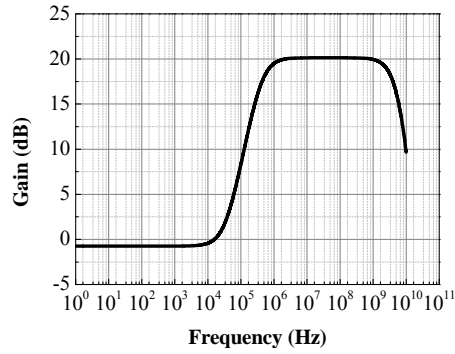
Fig.10. Transfer function of LA

C. Slicer

One of the most critical blocks in the receiver is Slicer. The circuit can be found in Fig.11. The main function of this block is to retime the data and make decisions every bit period [6]. In our design, the two-stage Slicer utilizes the clock provided by CDR to sample data streams. Under lock conditions, the rising edges of the clock are aligned with the data transitions while the falling edges of the clock sample the data in the middle of the symbol interval.
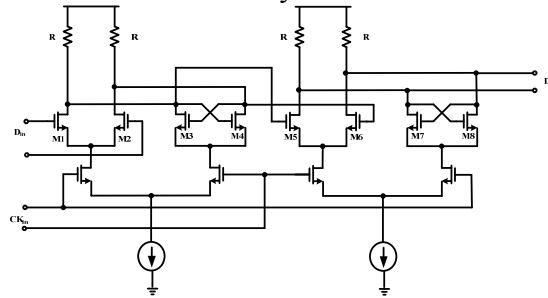

Fig.11. Slicer

Results

The layout is shown in Fig.12. Transceiver occupies die area about $1.68 \times 1.2 \text{mm}^2$. The transmitter and the receiver consume 72mW and 84mW, respectively, under a 1.2V supply. Meanwhile, PLL is under its own supply for separating.
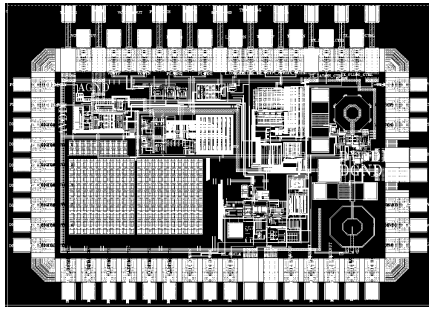
Fig.12. Layout of transceiver

A. Transmitter

Fig.13. (a) shows the output matching of the transmitter. Between dc and 2.5GHz, the transmitter's S22 is less than -15dB, suggesting little reflection. Fig.13 (b) depicts the eye opening of transmitter and illustrates transmitter can provide sufficiently large voltage swings for receiver while temperature rising from 0℃ to 60℃.

(a) S22 of transmitter   (b) Eye opening of transmitter
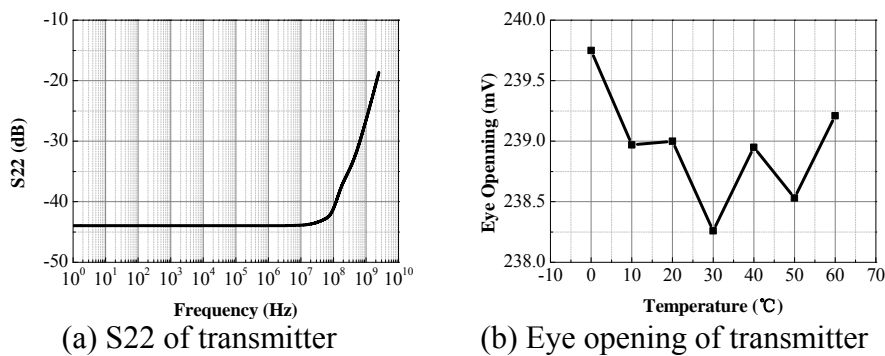Fig.13. Simulation of transmitter

B. Receiver

Fig.14. (a) illustrates the input matching of receiver. Between dc and 2.5GHz, the receiver's S11 is less than -15dB, suggesting little reflection. Fig.14. (b) depicts the peaking frequency of CTLE can set to 2.5GHz.

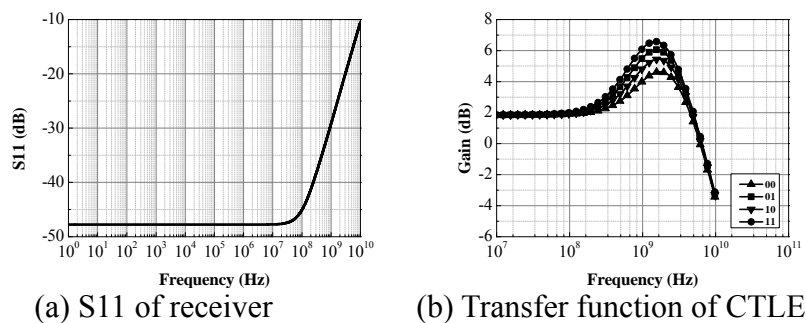(a) S11 of receiver   (b) Transfer function of CTLE
Fig.14. Simulation of receiver

Conclusion

In this paper, a 5-Gb/s transceiver is proposed. To compensate the loss of high speed data, 4-tap FFE is included in the transmitter and analog equalizers are utilized in the receiver. The 50-Ω single-end line terminations may be ac or dc coupled to the external line. To facilitate testing, PRBS generator and PRBS detector are integrated in the chip. The transceiver has achieved 5Gbps while

consuming 156mW under 1.2V supply. The proposed transceiver is well-suited for wire-line high-speed data transmission.

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