# The Design and Implementation of SCG H-bridge Unit Test System

Xia Fei, Huang Xiaobo, Xia Zongze

State Grid Liaoyang Electric Power Supply Company, Liaoning, China

Wang Yun

Beijing Institute of Mechanical Equipment, Beijing, China

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**Abstract.** SVG in distribution power grid has completely entered into the practical phase, as H-bridge of the core part of SVG, which is low test efficiency, poor reliability, high cost and requires repeated manual testing in the process of production. This thesis firstly analyzes the test environment of H-bridge unit, put forward the indicators, the overall design of testing system, puts forward the solution, then describes in detail the realization of the system hardware and software solutions, and finally through the chain H-bridge unit test, test the applicability of the system and work stability, this paper designed and implemented the SVG link test system has a broad application prospect.

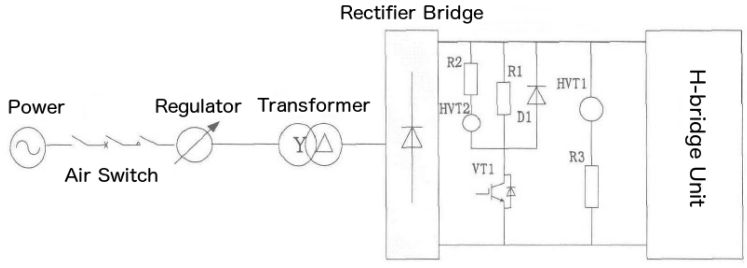
During 2001 to 2003, the United States put the large capacity SVG into use, and proved it has advantages in improving circuit transmission capacity, damping power oscillation, and enhance the system stability is superior performance, which shows that SVG has completely entered the practical stage in transmission- distribution power grid[1].

H-bridge unit, as the core module of SVG, its performance defines the overall performance of SVG system. To improve the quality of product and system safety in production, before the system put into use the performance test is deemed to undertake, the assemble can start once the test results satisfy the standard. A 35kv / 15mvar cascading SVG has 66 H-bridge unit need to be tested which require 66 times tests. As far as no H-bridge unit performance testing molding system exists, the test of H-bridge unit mainly rely on manual testing, which of low efficiency, poor reliability, high cost, difficulty in data storage, and waste of human resources. Therefore, to develop a set of reliable performance, flexible, easy to operate, suitable for a variety of voltage grade H-bridge unit test system is very meaningful [2].

## 1 H-bridge Unit Test Environment

### 1.1 H-bridge Unit Test Platform

H-bridge unit test platform is mainly responsible for DC side capacitor to H-bridge unit module provides a controlled dc power supply, its structure includes industrial power distribution cabinets, voltage regulator, transformer, three-phase rectifier bridge and its control and protection circuit, etc. After air switch closing, test platform getting power, by adjusting the voltage regulator changing the transformer three-phase AC output voltage to achieve the input DC voltage which can change the




DC side of H-bridge unit. The structure of H-bridge unit test platform is shown in Figure 1.

Figure 1. the circuit of test platform

The main parameters of H-bridge unit test platform are as follows:

Power supply:380V

Air switch:380V/400A

Voltage regulator: 40 kVA/ 50 Hz, self-coupled voltage-adjusting, input: 380 v, output: 0 ~ 430 V

Transformer: 200 kVA / 50 Hz, DY11 wiring, Ratio 400:3000

Rectifier bridge, three-phase rectifier bridge (3200 V / 270 A)

Test platform capacity: 200 kVA

**1.2 H-bridge unit**

H-bridge unit mainly includes five parts: DC capacitance, H-bridge circuit, DC power supply, controller and drive circuit, its structure is shown in Figure 2.

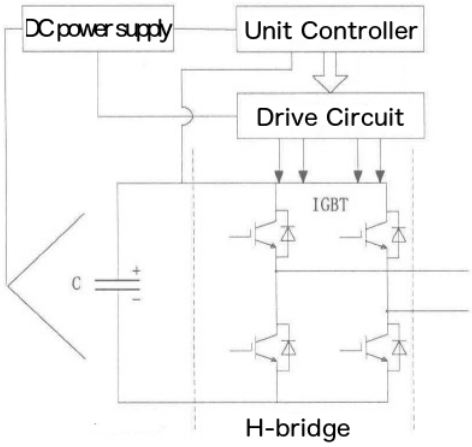



Figure 2. Internal structure of H-bridge unit

## 2 Design of H-bridge Unit Test System

According to the control requirements of cascading SVG system, there is some design requirements of the system performance in this test as follows:

(1)the SPWM modulation ratio must be set in the range of 5% ~ 95%.

(2) the SPWM carrier frequency, according to the cascading SVG system and the differences of different types of IGBT close frequency characteristic, can be selected as follows: 500hz, 600hz, 800hz, 600hz, 1000hz, 1500hz, 2000hz and other alternatives.

(3) the DC voltage in H-bridge unit has real-time acquisition and dynamic display, and display error is within 3%.

(4) Faults Display

To find the problems in the operation of the unit module, specific communication fault, such as DC over-voltage, IGBT overheat, SPWM wave fiber fault, + 24v power supply fault, H bridge driver fault, these faults must display the accurate positioning in real-time. And the communication failure, IGBT overheat fault, SPWM wave fiber fault, the failure of + 24v power supply, H bridge fault, required the test system to immediately stop SPWM wave sending, as to cancel the SPWM pulse for later transmit fault.

(5) Communication

Test system with H-bridge unit has two plastic optical fiber functioning as communication between modules, because the SVG system requirement for communication rate is 6.4K BPS, so the test system and communication between H-bridge unit must have a communication rate above 6.4 Kbps. The communication methods using in the test system is asynchronous serial communication.

(6) Human-Computer Interaction

Test system requirements has a real-time display H-bridge unit operation module, including H-bridge unit modulation, DC voltage, fault information, data, carrier frequency data and other information. Other information can also request by a peripheral module to change SPWM wave

modulation ratio, SPWM wave data such as carrier frequency, which can make the h-bridge unit work in different conditions.

**2.2 Design of the Test System**

The general design principle of the H-bridge unit test system is connecting four plastic optical fiber to H-bridge unit. Two of those four are using as communication and the other two are SPWM pulse transfer fibers. H-bridge unit transfer the information of running, direct voltage and malfunction to testing system. At the same time, the command and data from test system will also transfer to the H-bridge unit module through optical fiber. According to the requirements we mentioned above, the main function of the test system are human-computer interaction, SPWM wave creation and fiber communication[3].

The difficulty of this system is the design of SPWM wave modulated algorithm. Due to the control of the H-bridge by the main controller of cascading SVG device control system and using carrier phase shifting SPWM (CPS SPWM) system, the underlying H-bridge unit uses a single frequency doubling polarity SPWM modulation method, so the measured unit can provide a practical operation condition. Test system will also take a monopole frequency doubling SPWM modulation method.

Compared with the single polarity modulation and dual polarity modulation, Monopole frequency doubling SPWM modulation method can control algorithm simpler. High quality output voltage, low requirement to the output filter circuit parameters, four complementary switch tube, four switch tube fever and balanced life, high reliability of the circuit are also its advantages. Combined the actual requirement of SVG system of the test system, we can sure that SPWM modulation method of the test system is single frequency doubling modulation.

**2.3 Test System Solutions**

Test system based on ARM and CPLD H-bridge unit testing module, as shown in figure 3.

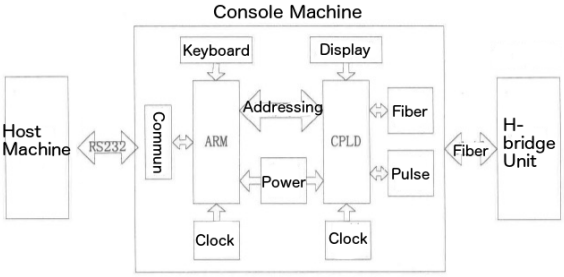



Figure 3. Program block diagram of test system based on ARM and CPLD

This scheme has the following advantages: make fully use of the control performance of the ARM and CPLD logic operation ability, and the host machine adopts a integrated touch screen with industrial computer, which can greatly reduce the volume and weight of the system, this host machine not only can satisfy the performance of the system, also will reduce the cost of the system, improve the portability of the system.

The host machine use the mcgsTpc embedded integrated touch-screen TPC7062K PC, adopts the MCGS embedded version of the configuration software development in Chinese. Configuration software MCGS embedded version has powerful functions and simple operation, easy to learn and easy to use. At the same time, the use of configuration software MCGS embedded version can avoid complex embedded version of the computer hardware and software problems, focus on the requirements and according to the characteristics of the engineering work, configuration of high reliability, high performance and highly specialized control monitoring system is needed.

Console machine with ARM and CPLD as the controller, among them, the ARM control the system and algorithm processing, CPLD is responsible for the timing sequence logic control and improve the cascading SVG H-bridge unit testing system of precision and data processing capacity.

H-bridge test system uses a monopole frequency doubling modulation method to control SPWM.

The whole system is divided into three units: human-computer interaction unit, system control unit and signal processing unit.

## 3 Hardware Implementation of the Test System

### 3.1 Function of Console machine

Console machine usually refers to a variety of data acquisition and monitoring equipment, they combined with other necessary equipment, gathering all kinds of parameters such as control as well as the state, and transform it into digital signal to the upper machine system. PC system to receive these signals, after will be in the form of appropriate such as images and sound to convey to the user, at the same time, the collected data are processed, inform the user equipment state of various parameters, then the processed data saved to the database, also can be transmitted to other monitoring platform through the network system, can also with other system constitutes a system function is greater. In addition, the machine can also directly to the operator's instructions, the signal is sent to PC, the control function of upper machine.

Master controller is a machine under the ARM single chip microcomputer STM32, coordinated controller is PLDEPM1270 Altera company.

### 3.2 The Structure of Console machine

The position machine system structure as shown in figure 4, including:

(1) Serial port communication module aim to realize host machine and console machine communication;

(2) Optical fiber communication module is implemented in console machine and H-bridge unit;

(3) ARM and CPLD in console machine communicate by eight address bus and 16 data bus to complete its parallel communication;

(4) ARM and CPLD in console machine connected with 2 10 roots optical fiber, which used as a data command transmision;

(5) ARM minimum system design including the power supply circuit, clocking circuit and reset circuit and JTAG circuit design;

(6) CPLD peripheral circuit design includes power circuit, clock circuit, the electric delay reset circuit and program download circuit design, etc.;

(7) The other circuit, including keyboard circuit, display circuit.

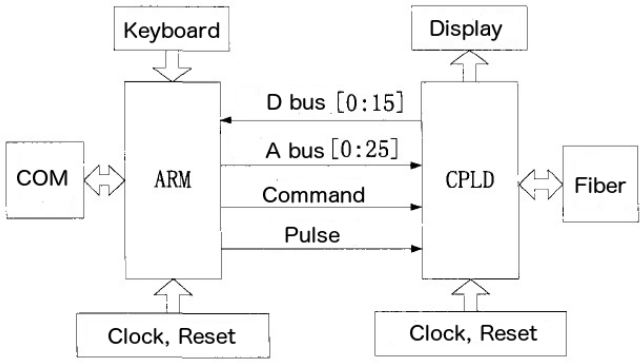



Figure 4. Overall structure of the console machine

## 4 Software implementation of Test System

### 4.1 ARM module

The design use ARM chip the STM32F103ZET6, software programming using Keil u Vision compile environment, choose C# as develop language [4], a machine system under the ARM of the program design is mainly to complete the five features:

(1) The integration between the touch screen industrial computer TPC7062K implementation and the host machine communication, including receiving message and returns, to complete the packet analysis and information extraction, including device address, function code, register address and data, etc.;

(2) According to the host machine data to generate the corresponding set of modulation ratio and carrier SPWM pulse signals, this process is to use a timer to capture interrupt and a sampling SPWM value calculation;

(3) Through external addressing, read the hypogyny machine of DC voltage and fault information code in CPLD storage;

(4) In the process of communication, there will be some specific interrupt program execution, such as sending and receiving USART interrupt;

(5) To ensure the accuracy of the content of the communication in the process of computing, from machine equipment to error detection, this design uses cyclic redundancy detection (CRC), it has the advantage of high detection efficiency, high detection accuracy.

Main program is the core of the whole ARM program. It mainly completes the system initialization settings, including RCC initialization, NVIC initialization, GPIO initialization, TIM initialization and USART initialization. After the initialization, software resets CPLD, reading memory cell data, estimating whether there is a module fault, releasing blockade pulse command if there is, estimating whether there is a serial port communication failures if there. Releasing blockade pulse command if there is, entering the rewards program, or else enter the return message module, then circularly reading the CPLD storage unit data, then enter return message module. The flow chart of ARM module process is shown in Figure 5.

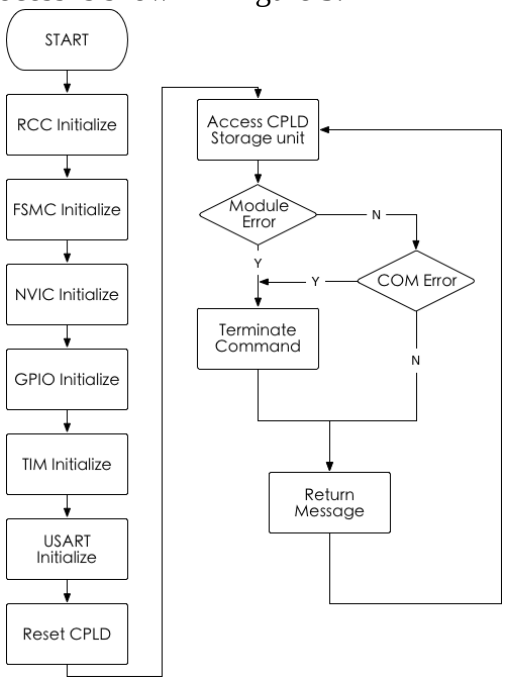



Figure 5. The flow chart of console machine ARM module

**4.2 CPLD program**

The chip used in this system is CPLD chip made by EPM1270T144C5N Altera company, compiled in QuartusII environment, using VHDL language. A machine system under CPLD programming has five features:

(1) complete serial asynchronous communication with H-bridge unit, complete H-bridge unit with message parsing and the extraction of information;

(2) Transfer ARM over the encoding command, complete the H-bridge unit test with optical fiber transmission;

(3) Encoding H-bridge units' DC voltage information and error log, put the encoding file in the storage unit, waiting for the acquisition of ARM;

(4) By monitoring ARM chips, the CPLD program will collect 10 ARM command information;

(5) Expand the 2 way SPWM pulse signals of the ARM to the 6 way pulse signals, so as to drive three H-bridge unit at the same time.

Console machine CPLD use asynchronous serial port communication with H-bridge unit CPLD, the bandwidth has been restricted to 648R/h. The process of CPLD applications described as follows: after power on, first initialize all registers, and then command H-bridge unit to reset, followed by parallel execution of three tasks: the first is the detection ARM's command, 10 compensation commands is executed on compensation, no compensation command is executed blockade, then the command code based on the communication protocol, was passed to H-bridge unit; The second is to receive a machine's message under DC voltage and fault information, the decoding in a storage unit, after waiting for ARM access, unlit fault information and the H-bridge light signal; The third is to ARM 2 SPWM pulse signals, forward and back to the 120 ° respectively, generates 4-way SPWM signal, then the SPWM signal through optical fiber to the unit is passed to the H-bridge, the specific flow of program design is shown in figure 6.

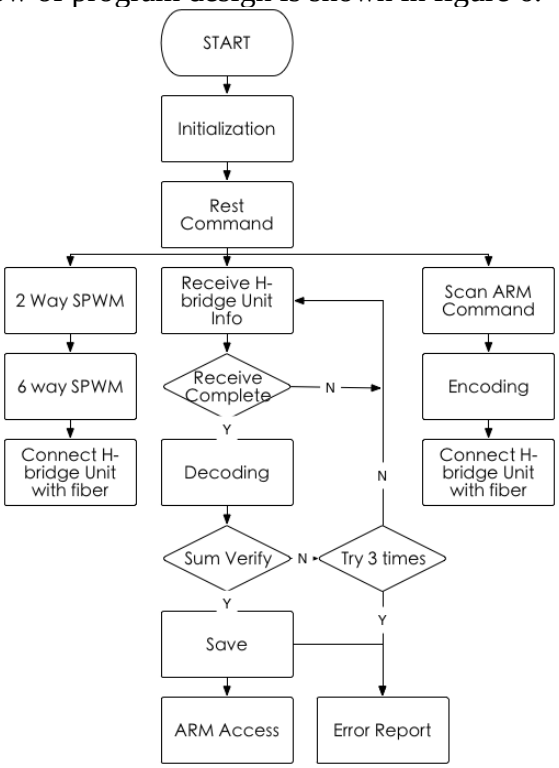



Figure 6. The procedure of console machine CPLD program

## 5 System Testing

The functional test of H-bridge unit adopts three series 230A/8.3mH reactor and they equal to a 230A/24.9.6mH reactor.

### 5.1 Rated Current Test

Connected to the power supply and test the load performance of H-bridge unit. Constantly improve the modulation ratio of the SPWM wave of H-bridge unit, then adjusting H-bridge output current to 200A, to get the rated current.

### 5.2 Heat Rum Test

Fan speed is 5 m/s and room temperature is 20°C. Operated the H-bridge unit under rated current for three hours and using temperature measuring gun to real-time monitoring IGBT temperature of H-bridge respectively in 30 min, 60 min, 90 min, 120 min. Table 1 shows the detailed test structure.

Table-1 Heat rum test record of H-bridge unit

| Recording Time（min） | Measured Temperature（°C） | Warming（°C） |
|---|---|---|
| 0 | 20 | 0 |
| 30 | 30 | 10 |
| 60 | 41 | 21 |

| | | |
|---|---|---|
| 90 | 47 | 27 |
| 120 | 52 | 32 |
| 150 | 55 | 35 |
| 180 | 58 | 38 |

### 5.3 Overload Capacity Test

Rising modulation ratio of SPWM wave of H-bridge unit and steady the output current to 1.1 times of rated current, which is 220A. Continuously running for 60s and we will have output current waveform of H-bridge shown in figure 8. Higher the the modulation ratio again and the current output will be 1.2 times of rates current which is 240A. Running for 10s and we will have the output current wave as we show in figure 9. Current is measured by Roche coil current. Graphic current value * 5 equals to actual current value.

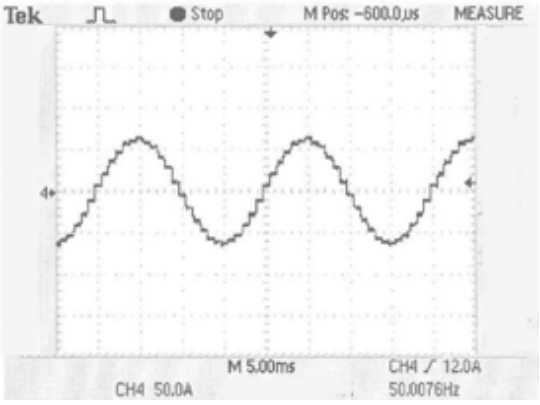



Figure 8. Output current waveform when the current is 1.1 times the rated current

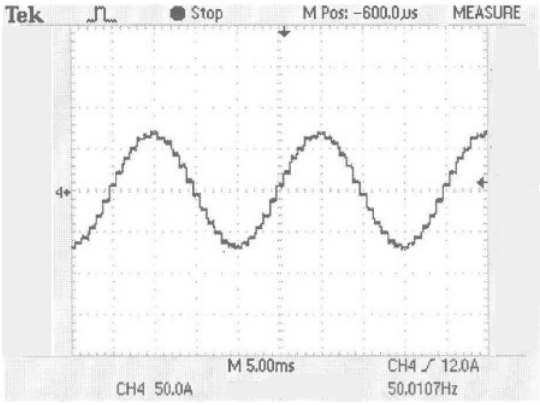



Figure 9. Output current waveform when the current is 1.2 times the rated current

## 6 conclusion

First, this paper analyzes the testing environment of the H-bridge and then come up with the index of the testing system. Designing the overall testing system and put forward the solution. After introducing the implementation scheme in detail, a confirmatory testing was conducted to see the applicability and working stability of the system by testing the H-bridge. The result shows that SVG H-bridge unit test system has a wide application prospect.

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