The Assessment and Analysis About the Superiority of VHDL Language on FPGA Design and Development

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Abstract. This paper is based on the effect that VHDL language on FPGA design and development, and we design the DDS module of FPGA by using the methods of designing. By research and analyse the The design of DDS module based on FPGA, we learn more about FPGA, visually and concretely. Also, We put forward the MidFilter based on VHDL language. The experiments show that the method can reduce deviation and improve the accuracy of the design.

1. Introduction

In recent years, integrated circuit and its design and manufacturing tools have been developed rapidly. The development of the CPLD（Complex Programmable Logic Device）and the FPGA（Field Programmable Gate Array）results in great changes of electronic design technology[1,2,3]. Because the FPGA program has short development cycle, low cost, high stability and the modified logic function, it's popular with the EDA(Electronic Design Automation) engineer. Then the need of electronic products based on FPGA is increasing. However, with the development of integrated circuit design technology and the enlargement of the design scale of the integrated circuit, the description methods of logic diagram and Boolean equation hardware become more and more complicated.[4,5] So there is a desire of a higher level modern design method and modern test method to describe hardware circuit.

The VHDL is the core of high-level design of digital system, and it is the key technology of new methods to accomplish digital system design. With the rapid development of Programmable Logic Device on speed and integration level, an increasing number of digital signal processing system can be accomplished by Programmable Logic Device. The digital filter is frequently applied by digital signal processing system. What's more, it is used to eliminate high frequency and cut down noise resulted from original(or input) sample data, and then get the needed output. This article puts forward a few optimized methods that design FPGA device using the VHDL. Using the technology of the parallel processing and assembly line of FPGA, the video image acquisition and processing system take up less system resources, and the processing speed is very high. Therefore, it has perfect practical value and application prospect.

2. Structure and Principle of FPGA

In the worldwide, the companies which produce FPGA devices are as follows: Xilinx, QuickLogic, Altera, Actel and so on. So the models and types of FPGA are different[7]. Although the function and specified structure of these FPGA devices have different advantages, their arrays are ordered by logic function blocks and these logic function blocks are connected by programmable interconnect resources, which are their common characteristics. The typical FPGA consists of the three kinds of resources: programmable logic function module, programmable input / output module, and programmable interconnect resources. The figure 1 shows their basic structure.

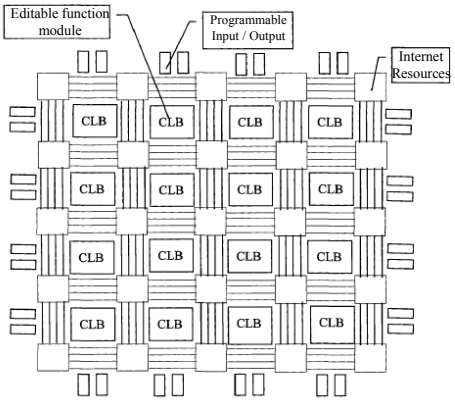

Fig 1. The Basic Structure of FPGA

The design flow of FPGA consists of design description, design input, design compilation, function simulation, time sequence simulation, allocation of devices and verification. The Chart 2 indicates the design flow of FPGA. By using the input methods of text , schematic diagram or the EDA , we analyze the function to be achieved of the designed system to design the input. During compiling, it points out the error so we can amend. The FPGA simulation divides into function simulation and time sequence simulation. After completing the simulation, we can let the design configure the target device to verify the hardware.

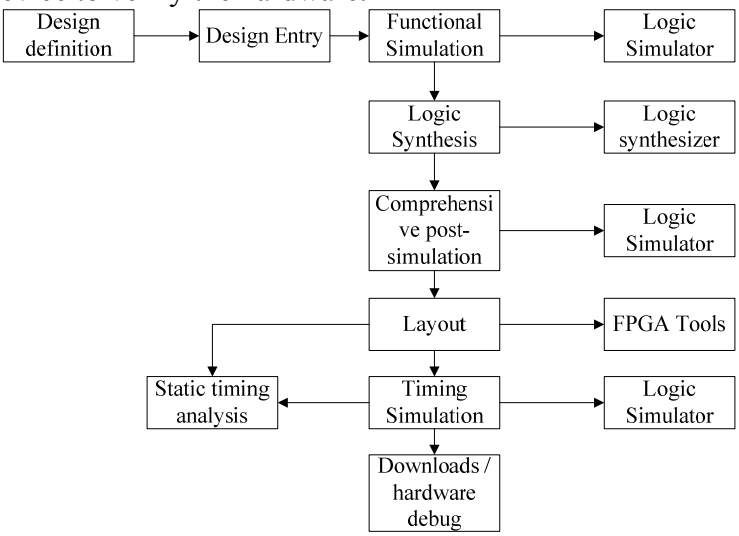

Chart 2. The Design Flow of FPGA

3.The optimized design method of VHDL

A complete VHDL program includes library, package, entity, architecture and configuration. The Chart 3 shows the basic structure. The entity and architecture are the basic parts of VHDL program and they compose the basic program of VHDL.

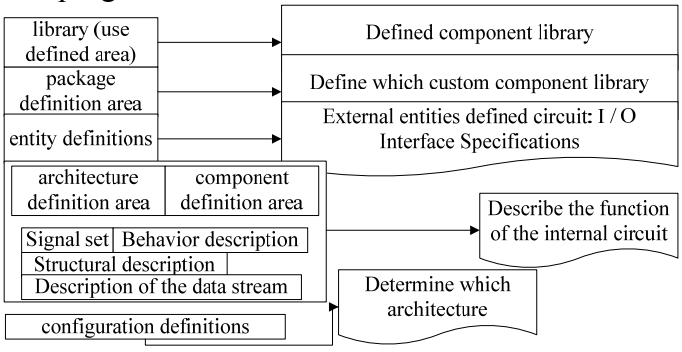

Chart 3. The Basic Structure of VHDL

The VHDL is a kind of behavior language. It allows designer to define the design in a higher abstract level, so the controls of resources and performance of the device are less. In the practice, we can use a lot of methods to compose VHDL code, and then optimize the design performance and improve the utilization of the device. Hierarchical design is a very simple skill. Many design's functions are very complicated and they can't achieve in a same design file. So the designer can use standard VHDL module to set up the design rather than optimizing the whole design. The division of design level should be made according to function boundaries and make the I/O connection of the modules minimum. After completing a hierarchical design, the designer can pass option setting in developing tools. When they design a combined logic, the designer should avoid forming a latch unconsciously due to the design style. For example, when "case" or "if" sentences can't cover all possible conditions completely, the combination may form a latch. To lessen the condition that the signals of critical path delay, the designer can use "if" sentence to make priority code. The FPGA is measured the circuit area by logic unit, so the synchronous design doesn't waste more resources than asynchronous design. When considering the delayed design, the delay of asynchronous circuit can achieved by the gate delay, so it is more difficult to predict. The synchronous circuit achieves delay by using counter or trigger. The quality and stability of signal depend on the performance of the sequential circuit.

4. The IC design based on VHDL language

4.1 The design of DDS module based on FPGA

This system uses the chip EP2C8Q208C8 of Cyclone II series produced by Alter company to design DDS module. As a chip with higher cost performance and compared with the first generation of EP1C6 or EP1C12, the Cyclone II series chips improve a lot in design and inside logic resources, and its price is accepted by those electronic enthusiasts. This system makes full use of its advantages and use DDS principle to design DDS module based on FPGA, whose top document are shown by Figure 4. The module includes phase locked loop circuit, interface circuit between single chip microcomputer and FPGA, phase accumulator and ROM.

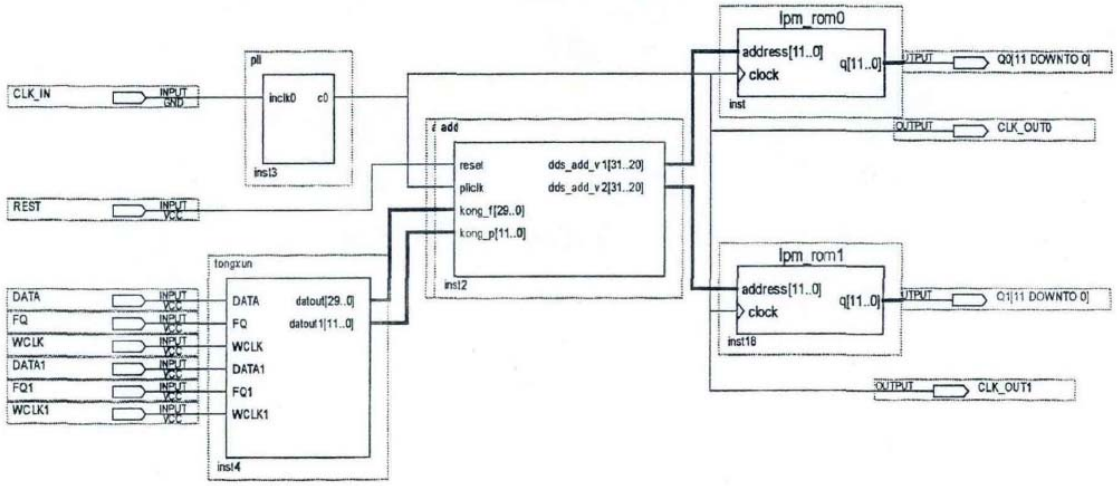

Fig 4. The Symbol File of DDS module

The word length of this system's phase accumulator is 32 bits, the reset signal has the function of resetting. When the signal is 1, the phase accumulator accumulates one time based on K in a clock cycle. Select the address bus of higher 12 bites to connect the ROM. The description language structure of the hardware is:

```
ARCHITECTURE abc OF add Is
SIGNAL dds add :std_logic_vector(31 DOWNTO 0); ——DDS address accumulator.
SIGNAL dds m : integer RANGE 1 TO 1073741824 ; ——dds frequency register
SIGNAL dds n : integer RANGE 0 TO 4096 ; ——dds phase register
——**********DDS address accumulator process**********
BEGIN.
```

```
PROCESS(reset，pllclk)
BEGIN.
IF reset= ' 0'   then
dds_add<=(OTHERS=<”0”) ;
  ELSIF (pllclk’EVENT   AND   pllclk=’1’)   THEN.
      ——DDS accumulator accumulates circularly   dds m.
  IF dds add<4294967296 THEN
         dds add<= dds_add+dds m;
  ELSE.'
  dds_add<=dds_ add+dds_m~4294967296;
          END IF;
      END IF;
  END PROCESS;
 dds_m<=CONV_INTEGER(kong_f );
 dds_n<=CONV_INTEGER(kong_p );
 dds_add_vl<=dds_add(31 DOWNTO 20);
 dds_add_v2<=dds_add(31 DOWNTO 20)+dds_n;
 END abc;
```

Considering the smoothness of output signal and the internal resources of FPGA, this system design 4096 sampling points as a cycle, so they use two RONL of 12 bits(4096 bytes), whose Symbol File is shown by Chart 5.

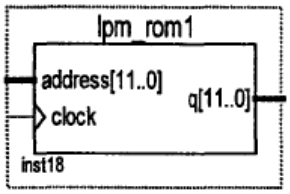

Chart 5. The Symbol File of ROM

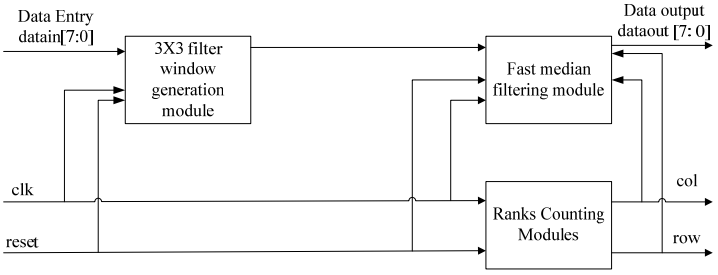

Chart 6. The median filter structure of fast speed

5. The Proposed Algorithms of Median Filtering

When the filter window is 3×3, it needs read 9 pixel data from continuous 3 lines, the brightness of the pixel is stored equally in the lower 8 bits of SRAM. So we only need read the lower 8 bits of memory cell, that is the component of brightness, to get a gray picture. The overall design scheme is shown by Chart 6.

The median filter structure of fast speed consists of 3×3 filter window generation module, median filter module of fast speed and the row counter module. The data is input from datain[7:0], and the dataout[7:0] is the output value. The clk is the clock signal of system, the reset is the resetting signal, col and row is the position of current processing pixel.

When we use this algorithm to achieve the order filter circuit, we need an order comparator of three input signal to order the three elements. The core code of VHDL of order comparator is shown as follows.

```
if(dinl<din2)then
minvar:=dinl:
medvar:=din2;
e1se
minvar:=din2
medvar:=dinl
endif;
if(din3<minvar)then
maxvar:=medvar;
medvar:=minvar;
```

```
minvar:=din3;
else if(din3<medvar)then
maxvar:=din3;
else
maxvar:=medvar;
medvar:=din3;
endif;
min:=minvar;
med:=medvar:
max:=maxvar.
```

Chart 7 is the structure of median filter algorithm, the XYZ is three input comparator, the XY is bidirectional input comparator. The input of comparator is the gray levels of a row of pixel. The three input signal comparators of the first line accomplish the order of a series of data in the clock cycle, and the three input signal comparator of the second line compare the median of the three ordered lines. The three input signal comparators of the third line order the three ordered lines again according the results of the second line. The two lines complete that in a same clock cycle. Then, this text compared the maximum of NO.3 with NO.4 and chosed the maximum of the bidirectional input comparators in the forth line. At the same time, the bidirectional input comparators in the forth line chosed the the minimum, which compared the NO.5 with NO.6. Both of these two comparators could also be completed in a same clock cycle. Finally, there is a three-input signal comparator in the last line, it compares NO.5 value with the former two values, and the value is exactly the final median value of filter window.

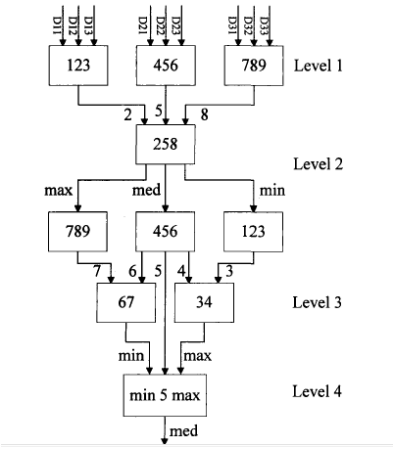

Chart 7. The structure of median filter algorithm of fast speed.

6. Experiment's design and development

By the design scheme of system, engineers will design a detailed circuitous philosophy diagram firstly and then draw a printed circuit board of PCB. Use the digital oscilloscope whose model is Gwinstek GDS-2102 l00MHz Digtal Storage Oscilloscope and keep the output signal frequency the same. Then the push-button sets different phase difference. What's more, we detect and record the actual output phase difference, then establish the Table 1.

Table 1. Phase-shifting data (frequency f=1kHz, no load)

Presetting phase-shifting/degree	Measured phase-shifting/degree	Error
30	30	0
45	45	0
90	90	0
145	145	0
180	180	0
270	270	0
300	300	0
330	330	0

Using a high precision frequency meter to measure the frequency of waveform output by system and then establish the Table 2. From the data in the table we can see that the frequency error of waveform output by system is very small, and it achieves the system's requirements fully.

Table 2. The test data of frequency (phase-shift 180°, no load)

Presetting frequency/HZ	Measured frequency/HZ	Error/%
1	1.0002	0.02
100	100.011	0.011
1000	1000.03	0.003
5000	5000.05	0.001
10K	10.0002K	0.002
50K	50.0025K	0.005
100K	100.002K	0.002
1M	1.00014M	0.014

7. Conclusion

Based on the analysis of superiority of Programmable Logic Device and VHDL language on the design and development of FPGA, we've accomplished the design of DDS module based on FPGA. What's more, we do a simulation towards median filter algorithm and use VHDL language to complete it in the internal of FPGA. In the environment of compiling, we simulate the process of producing the driving signal and do an error analysis towards the whole system's function. As a result, we know that VHDL plays an important part in FPGA design. And the accuracy of the design can be improved and the error of the whole system lessend by this paper.

Reference

[1] YUAN Chunfeng, ZHANG Zesheng, CAI Xiaoyan. 《Teaching Reform of the Principle of Computer Organization Lab Course 》 《Computer Education.》 2011.10 Page 110-114

[2] GONG Jian. 《The Image Process System Based on FPGA》Wuhan, Wuhan University Of Technology 2007，p2-3

[3] BAO Bengang. 《Implementation of a Complete Synchronization Digital Frequency Meter Based on FPGA》 Changsha, Hunan University. 2007:1-17, Page 43-44.

[4] GUO Haiqing. 《The Analyses of Improving the Measuring Accuracy by Electronically Count Measuring the Frequency》 《Journal of Qinghai Normal University(Natural Science Edition)》 2009, Page 10.

[5] YANG Shouliang. 《Construction and Realization of the Digital Cymometer Based on FPGA》. Modern Electronics Technique 2005, Page 11

[6] WANG Xudong, PAN Guangzhen 《MATLAB and Its Application in FPGA》Beijing, National Defence Industry Press, 2006.

[7] SUN Chengzhi, XIE Mei 《Design of Image Acquisition Unit Based on FPGA》 Microcontrollers & Embedded Systems 2008, Page 51-53.